Low Power Test Pattern Generation of Logic Built in Self Test

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Abstract:- Power,area and time are the major challenges for VLSI circuits.Power consumed during scan based test mode is much more than in normal mode because of increased switching transitions.This work aims to reduce the switching transitions and power dissipation of Logic Built In Self Test(LBIST) which produces a pseudo-random test patterns.LBIST tests the functional logic of a chip in similar way like Memory Logic Built In Self Test(MBIST).In this paper,we propose a low power pseudo random test pattern generator(PRPG) with test compression capabilities of LBIST for test applications with desired fault coverage and toggling levels. A low power PRPG comprises of linear feedback shift register(LFSR) drives along with a phase shifter and combines with other features and device produces binary sequences with preselected toggling (PRESTO)activity and the output of phase shifter is taken into transition controller which reduce switching transitions.Furthermore, the proposed system is simulated using Mentor graphics HDL designer2012.1 and the results are obtained and compared with existing technique.

Keywords:Logic built in self test(LBIST),Memory built in self test(MBIST),transition controller,Linear feedback shift register(LFSR)

I.INTRODUCTION

Over the decade of years,the main objective of manufacturing test remains same to ensure reliability and high quality semiconductor products.To overcome the disadvantage of growing test volume and test data bandwidth we introduce a hybrid approach of combining LBIST with test compression.LBIST is mainly devolpedfor board,system and in-field test.Differnt test patterns are generated using different BIST schemes and switching activities and power dissipation is reduced[2],[3],[13].As with conventional scan- based test more power is consumed with high date activity compared with circuit-under test.Power induced during scan based test results in thermal issues,voltagenoise,power drop or excessive peak power which causes a yield loss due to device damage which decreases chip reliability,reduces lifetime or a device malfunction following delay increase.Numerous power reduction schemes has been devised,[5]among them there are specific techniques proposed for BIST to keep peak power below a given threshold.Forexample,test power is reduced by preventing transitions at memory elements from propagating to combinational logic during scan shift[9].this is achieved by inserting gated logic[10] between scan cells outputs and logic they drive.A synergistic test power reduction[8] method and a test vector inhibiting scheme of mask test patterns generated by an LFSR has been proposed.Elimination of such tests can reduce switching activity with no impact on fault coverage.

The emergence of low-transition test pattern generators[6],[4]added a new way to power aware solutions.Depending on the number of inputs, a dual-speed LFSR[12] which consists of two LFSRs which is driven by normal and slow clocks which reduces the switching activity in the circuit.Then,a gated LFSR clock[14] has been

proposed to reduce power consumption.combining low transition generator with a weighted pseudo random generator can also reduce switching activity.

II.BASIC ARCHITECTURE

A n-bit PRPG is connected with a phase shifter feeding scan chains producing pseudo random test patterns.A linear feedback shift register(LFSR) or a ring generator can implement a PRPG.In between PRPG and phase shifter n hold latches are connected and it is controlled by n-bit toggle control register.When the enable input is given, the latch becomes transparent otherwise latch is disabled and captures and saves for a period of clock cycles with constant value feeding phase shifter.

The toggle control registers supervises hold latches which consists of 0s and 1s where 1s indicate toggle mode thus latch is transparent for data moving from PRPG. The toggle control register are loaded once per pattern count with additional shift register content and the enable signals for the shift register are produced in probalisitic manner by using original PRPG with programmable set of weights.The weights are determined by four AND gates producing 1s with probability 0.5,0.25,0.125,0.0625 respectively.the OR gate allows choosing probabilities beyond powers of 2.

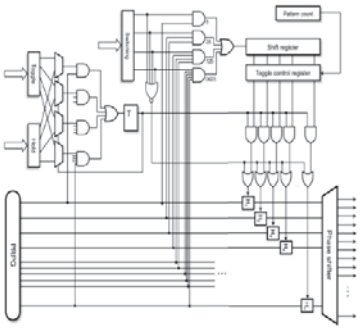

Fig1:Operational version of PRESTO generator

An additional 4-input NOR gate detects the switching code0000, which is used to switch the LP functionality off.So,while working in weighted random mode,the switching selector ensures stastically stable content of the control register interms of amount of 1s it carries.Much higher flexibility in forming low-toggling test patterns can be achieved using this architecture.This approach splits up a shifting period of every test pattern into sequence of alternate toggle and hold intervals.To move to and forth between toggle and hold states,we use a T-flip flop that switches wheneverthere is at 1 on its data input.If it is set to 0,the generator enters in hold mode with temporarily disabling latches regardless of the toggle control register.If it is set to 1,it enables the latches and enters into togglemode which moves data from PRPG to scan chains.

Two additional parameters kept in toggle and hold register determine how long the entire generator remains either in toggle or hold mode.To terminate either mode,a 1must occur on T-flip flop similar to that of a weighted logic used to feed the shift register.The T-flip flop controls four 2-input multiplexers routing data from toggle and control registers.It allows selecting a source of control data that will be used in the next cycle to change the operational mode of the generator.testpatterns.When using the PRESTO generator with existing DFT flow,all LP registers are either loaded once per test data registers or parts of an IJTAG network,and are initialized by the test setup procedure.Clearly,it suits LBIST applications where shift speeds are quite high.

III.EXISTING SYSTEM

A.Automatic selection of controls:

As shown in operational version of PRESTO generator depend on mainly three factors in BIST mode they are:1)1the switching code(kept in switching register 2)the hold duty cycle(HC) 3)the toggle duty cycle.Given the size of PRPG,the number of the scan chains and the corresponding phase shifter, the switching code as well as HC and TC values can be selected automatically in such a way that the entire generator will produce pseudorandom test patterns having a desired level of togglingT provided the scan chains are balanced.The procedure for selecting these parameters consists of many steps and values of switching hold and toggle codes yields a ratio r with smallest deviation from theoretical values using equation A=(T * S)/50 where S is the total number of scan chains and T is the toggling level (%) and A is the number of active scan chains.

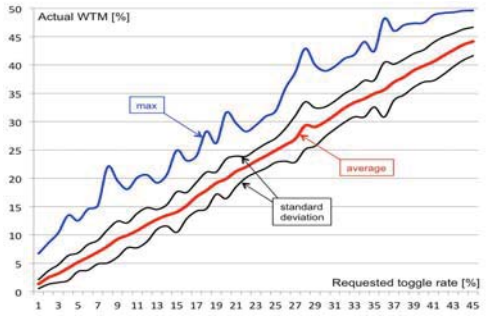

Fig 2: Toggling(WTM) for the five designs and 33-bit PRPG

b.LPdecompressor with ring generator:

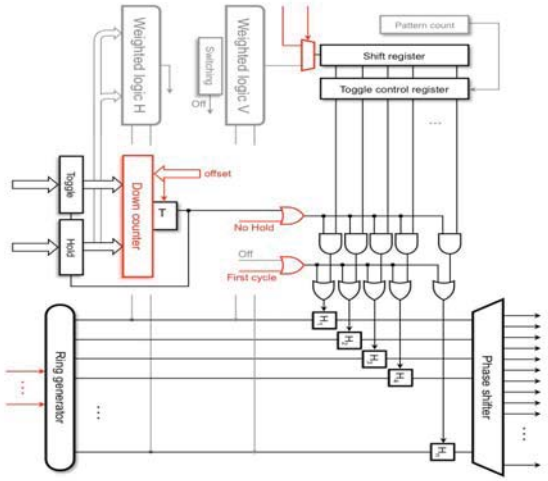

Fig 3:LPdecompressor with ring generator

1.Ring generator:

Ring generators are high performance LFSR which produces pseudo random test patterns which produces binary sequences.Two adjacent flipflop contain atmost one 2-input XOR gate and each flip-flop output drives atmost 2 fanoutnodes.The circuit is constructed in ring structure so there is no long feedback path connecting the right most

flipflop to the left-most flip flop.It is a ring shape structure and produces two layer feedback so power consumption will be more.

The principle of thedecompressor is to disable both weighted logic blocks(V and H) and to deploy control data instead. The content of toggle control register can be selected in deterministic manner due to multiplexer placed in front of shift register.Further, the toggle and hold registers alternately preset a 4-bit down counter, thus determine the durations of hold and toggle phases.When circuit reaches a value of zero, it causes a dedicated signal to go high in order to toggle the T-flip flop.The same signal allows the counter to have the input data kept in toggle or hold register entered as the next state.

Both the down counter and the T-flip flop needed to be initialized for every test pattern.The initial value to the T-flip flop decides whether the decompressor will begin to operate either in toggle or in the hold mode, while the initial value to the counter is reffered to as an offset, determines mode's duration.The functionality of the T-flip flop remains same as that of LP PRPG.Here, it occurs in two cases: First of all, the encoding procedure can completely disable the hold phase by loading the Hold register with appropriate code.If detected (No Hold) it overrides the output of the T-flip flop by using an additional OR gate.As a result, the entire test pattern is going to be encoded within toggle mode exclusively.In addition ,all the hold latches have to be properly initialized.Hence a contro signal First cycle produced at the end of ring generator initialization phase reloads all latches with current content of this part of the decompressor.

IV.PROPOSED SYSTEM

In order to facilitate test data decompression while preserving its original functionality the circuit is rearchitected.This architecture consists of an additional block transition controller and ring generator is replaced by LFSR.LFSR produces pseudorandom test patterns and consumes less power compared to ring generator.Transition controller produces less controlled transitions on phase shifter outputs.

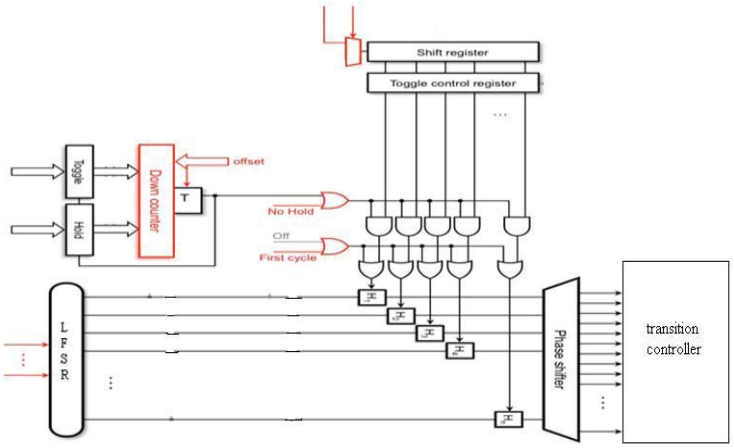

Fig 4:LP decompressor with LFSR and transition controller

1.LFSR:

In the proposed system, Linear feedback shift registers(LFSRs) produce extremely good pseudorandom test patterns.Gated clock signal present in design approach for LFSR lead to power reduction.Power reduction hardly depends on technological characteristic of gates employed.LFSR is a shift register whose input isresult of XOR of some of its inputs.The outputs of flip-flops are loaded with seed value(anything except 0s which cause LFSR to produce all 0 patterns)and when LFSR is clocked,it will generate PRPG of 1s and 0s.Here,the signal necessary to generate test patterns is clock.Maximum length of LFSR is 2^n-1.

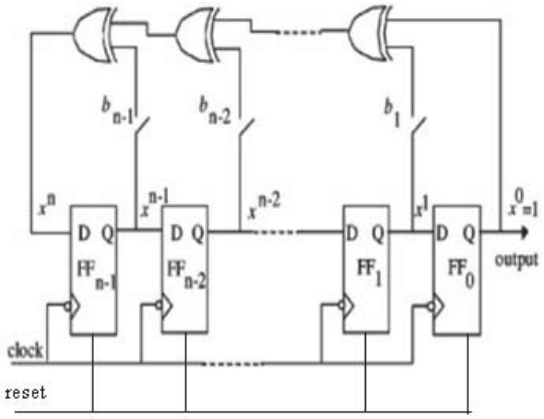

Fig.5: Simplified circuit of a generic LFSR circuit

2.Low Power PRPG architecture with transition controller:

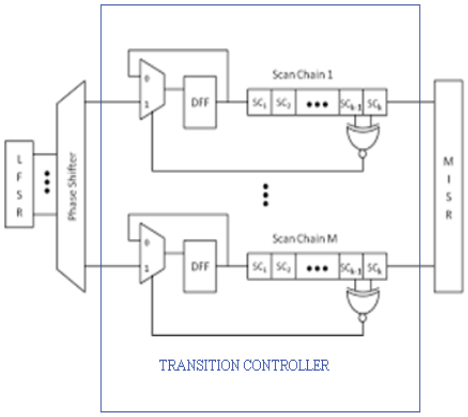

Fig 6: Low power PRPG with transition controller

An adaptive technique is applied to reduce the shift power to improve the shift power reduction in logicBIST.To get the required power reduction, we implement an additional module called transition controller.During shift mode the previous test responses in scan flip-flops are given as feedback to transition controller which is used to generate test patterns so that switching is reduced.

The transition controller consists of a multiplexer,a XNOR gate and D-flip flop.The inputs of XNOR gate is driven by the outputs of last two scan cells in the same chain SCk-1 and SCk.The output of XNOR gate connects to multiplexer selects input and here,we assume that there is no inversion between SCk-1 and SCk.When SCk-1 and SCk have different values ,the value at XNOR gate output is 0 and it causes the D-flip flop hold its previous value.Otherwise the D-FF will be updated by phase-shifteroutput.

Cycle	Scan Chain Value	No Transition Controller		With Transition Controller			
		Scan chain values	*Tr.*	*Scan chain values*	*XN OR*	*FF o/p*	*Tr.*
-	001010	011001	-	011001	0	0	-
1	00101	001100	6	001100	1	1	6
2	0010	100110	9	100110	0	1	9
3	001	010011	11	110011	1	1	6
4	00	101001	13	111001	0	1	4
5	0	010100	14	111100	1	0	2
6	-	001010	10	011110	0	0	6
Total			63		33		

Table 1:Comparison of BIST units

Table1 shows the process of shifting test pattern with and without transition controller of BIST units with assumed test pattern as 001010.It is obvious that the number of transitions is reduced from sixty three to thirty three.

IV.RESULTS AND DISCUSSION

The efficiency of the work is analyzed using S27 benchmark circuit of ISCAS'89 family.Mentor graphics HDL designer 2012.1 and Xilinx are the tools used for simulation and interpretation. Scan chain is formed with the flip-flops from S27 circuit.

Simulation result of ring generator ,LFSR,PRESTO ring generator and LP decompressor are discussed.

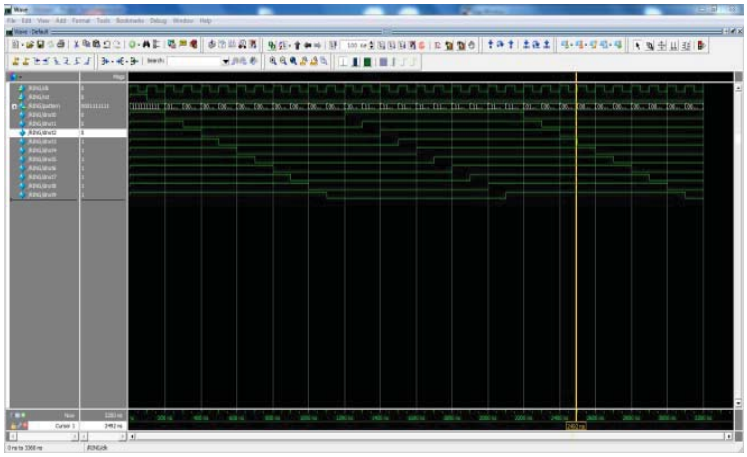

Fig 7:Simulation result of Ring Generator

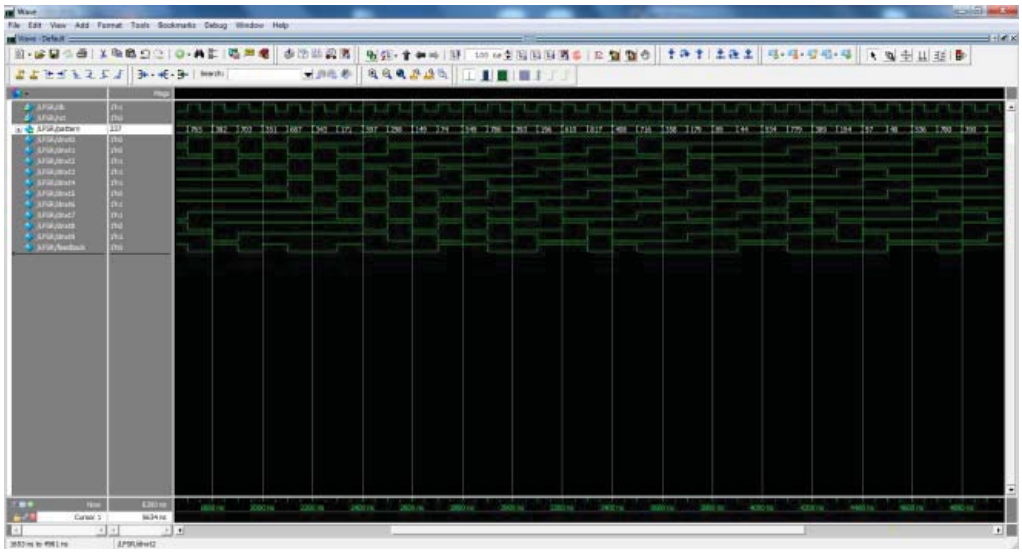

Fig 8:Simulation result of LFSR

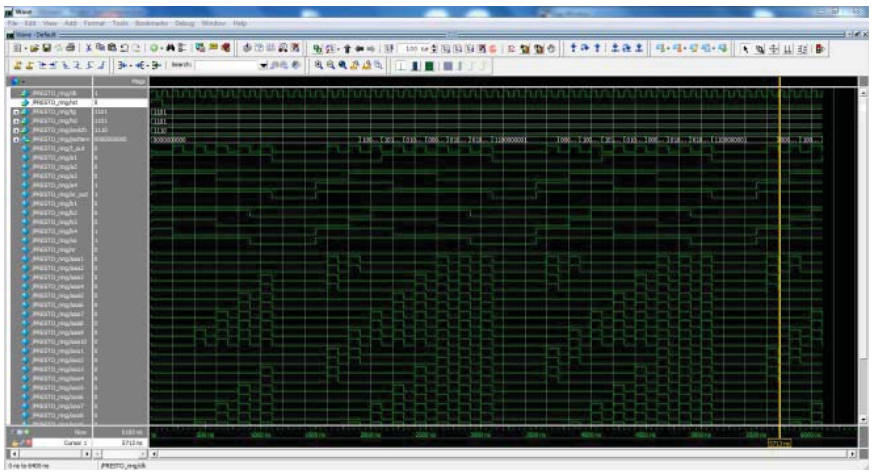

Fig 9: Simulation result of PRESTO ring generator

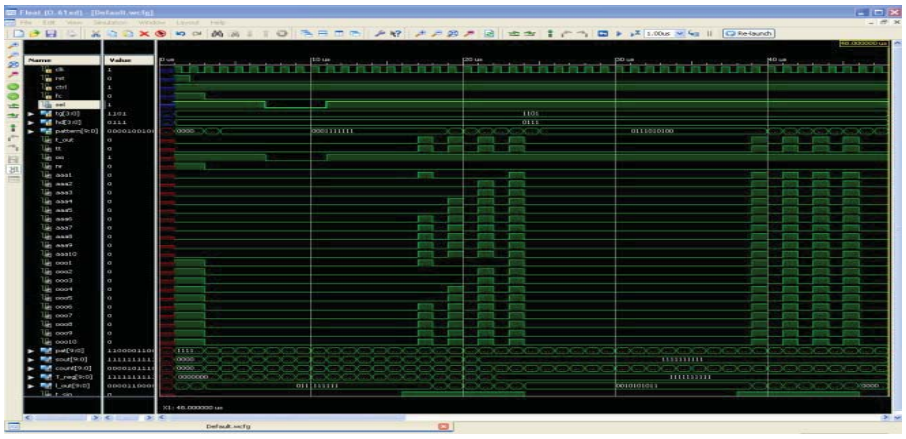

Fig 10:Simulation result of LP decompressor

S.No	Test pattern generation and compression techniques	Power consumption
1	PRESTO ring generator	0.344W
2	LP decompressor with LFSR	0.240 W

Table2:Comparison of ring generator and LFSR

V.CONCLUSION AND FUTURE WORK

Using LP decompressor with LFSR, pseudo random test patterns are generated with reduced switching activities so that power dissipation will be reduced.We have compared power dissipation of LP decompressor with LFSR and PRESTO ring generator.Further,we introduce a block called transition controller which further reduces power dissipation in future.

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