System Level Design and Layout Abstraction of On-Chip High Voltage Generator

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Abstract- This paper presents that system level design for on-chip high voltage generator. High voltage generator produces the output voltage which is higher than the input supply voltage with the help of charge pump circuit. This high voltage is widely used in memory applications (such as EEPROM, MNOS, FLASH MEMORY, and ENERGY HARVESTERS) for read or writes operation. Output voltage depends on the number of stages present in the charge pump circuits. This paper includes the layout abstraction for on-chip fabrication.

I. INTRODUCTION

The high voltage generator circuit consists of three blocks. First is a clock driver circuit, which contains an oscillator and a non-overlapping clock. Second is a charge pump and the third is voltage regulator, which is composed of a divider, a comparator and a band gap reference. The on-chip oscillator generates the 5 MHz clock. Non overlapping clock produces a two-phase clock which is used by the charge pump clock driving terminals. The charge pump produces high voltage by pumping charges from the supply voltage to high voltage. The divider and comparator can stabilize high voltage and produce a feedback signal.

II. PROPOSED METHOD

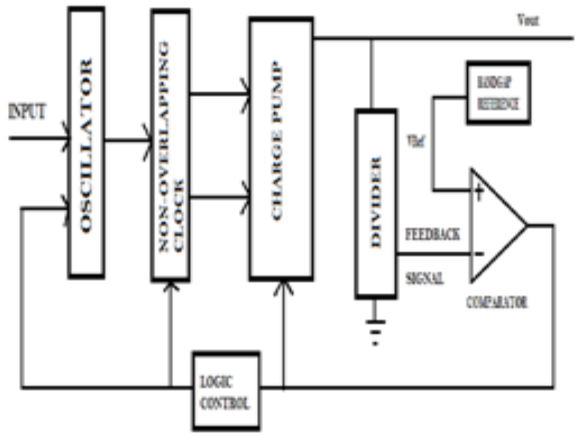


fig a.proposed method

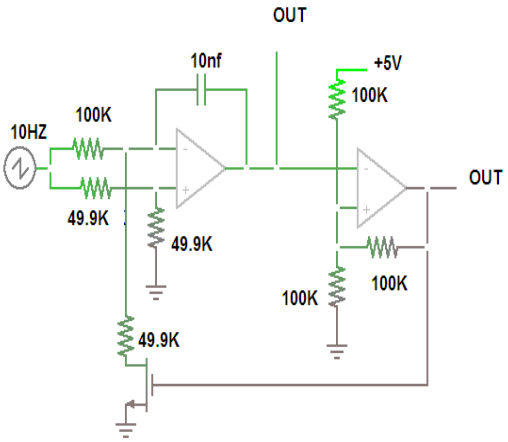


fig b.oscillator

This circuit is a voltage-controlled oscillator, which is an oscillator whose frequency is determined by a control voltage. A 10 Hz saw tooth oscillator provides the control voltage in this case; this causes the frequency to rise slowly until it hits a maximum and then falls back to the starting frequency.

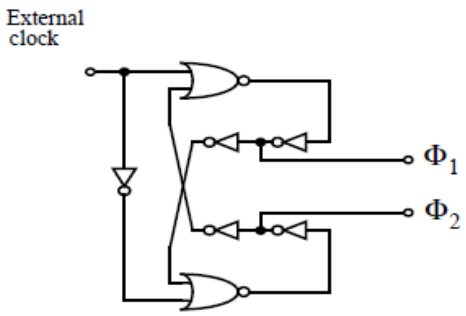
The first op-amp is an integrator. A voltage divider puts the + input at half the control voltage. The op-amp attempts to keep its – input at the same voltage, which requires a current flow across the 100k to ensure that its voltage drop is half the control voltage.

When the MOSFET at the bottom is on, the current from the 100k goes through the MOSFET. Since the 49.9k resistor has the same voltage drop as the 100k but half the resistance, it must have twice as much current flowing through it. The additional current comes from the capacitor, charging it, so the first op-amp must provide a steadily rising output voltage to source this current.

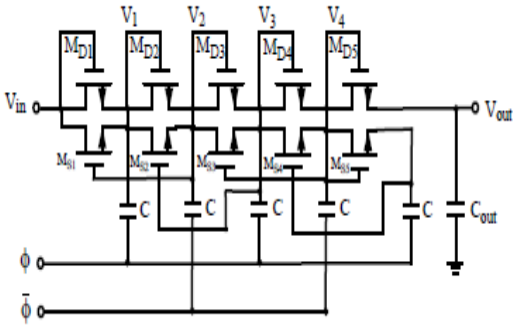
When the MOSFET at the bottom is off, the current from the 100k goes through the capacitor, discharging it, so a steadily falling output voltage is needed from the first op-amp. The third scope shows the output voltage; it looks like a triangle wave.

The second op-amp is a Schmitt trigger. It takes the triangle wave as input. When the input voltage rises above the threshold of 3.33 V, it outputs 5 V and the threshold voltage falls to 1.67 V. When the input voltage falls below that, the output goes to 0 V and the threshold moves back up. The output is a square wave. It's connected to the MOSFET, causing the integrator to raise or lower its output voltage as needed.

NON OVERLAPPING CIRCUIT

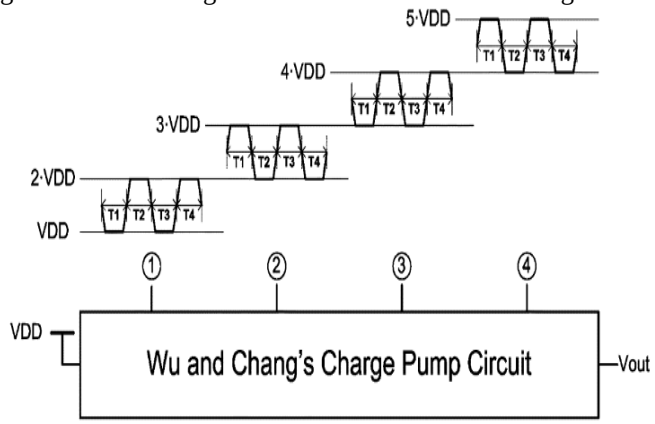


CHARGE PUMP CIRCUIT



The full swing clock signals and were generated from an integrated, non-overlapping, two phase clock generator. A non overlapping clock that produces a two-phase clock is used to drive the charge pump clock terminals.

Charge pumps employ dynamic switches to increase the voltage pumping gain. The MOS switches with precise on/off characteristics to direct charge flow during pumping rather than using diodes, or diode connected transistors which inevitably introduce a forward voltage drop at each node.
The operation of this new charge pump is identical to the operation of the Dickson charge pump and the same initial voltages will be established at each pumping node.
The four-stage charge pump circuit is reported by Wu and Change. The charge transfer switch (CTS) controlled by the dynamic control circuit in the Wu and Change charge pump circuit is used to transfer the charges from the present stage to the next stage without suffering the limitation of threshold voltage.



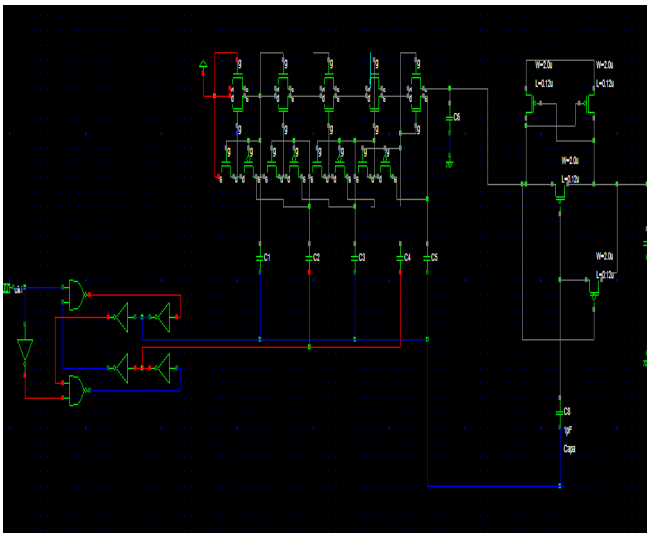
(b)

The corresponding voltage waveforms of the four-stage Wu and Chang charge pump circuit**.** When the clock signal CLK is low and the clock signal CLKB is high during the time interval T1, the voltage on node 1 is VDD and the voltage on node 2 is 3 X VDD. Because transistor MN1 is turned off and transistor MP1 is turned on, the charge transfer switch, MS1, can be completely turned on to transfer charges from the power supply (VDD) to node 1. During the time interval T2, the voltage on node 2 can be pumped as high as 2 X VDD to turn on transistor MN1 and to turn off transistor MP1. Thus, the charge transfer switch, MS1, can be completely turned off to prevent the charges back to the power supply (VDD). The operation of next stages in Wu and Chang's charge pump circuit is similar to that of the first stage. Because the CTSs can be completely turned on or turned off by the dynamic control circuits, the pumping efficiency has been enhanced with ideal output voltage of 5 X VDD.

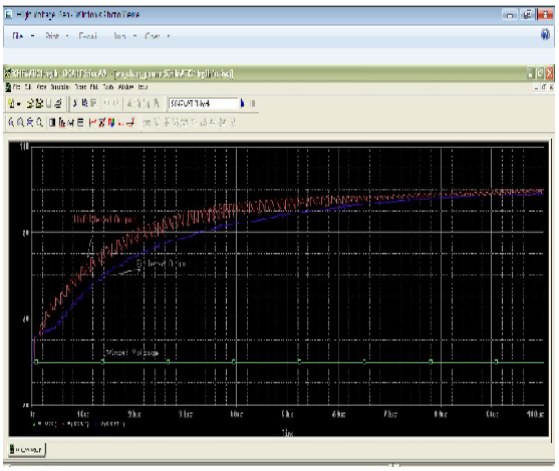
III. VOLTAGE REGULATOR

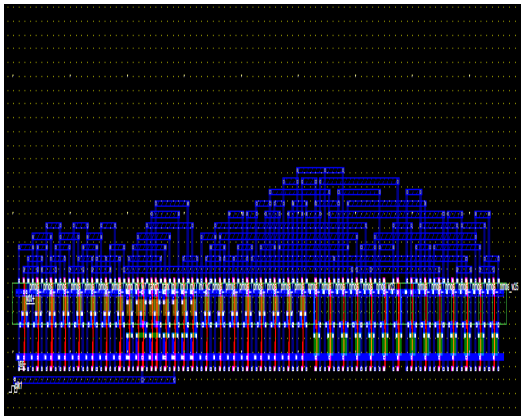
To stabilize the high voltage and reduce the power consumption, a voltage regulator is used. When the feedback signal produced by the band gap reference reaches higher than Vref, the comparator and logic control circuit work together to turn off the clock. Similarly, when the feedback signal is lower than Vref, the comparator and logic control circuit work together and continue driving the clock and charge pump. Vref is determined by VDDHV and the value is 1.5 V. By controlling the on/off of clock and charge pump, low power is obtained. Furthermore, when a capacitance divider is applied, there is no current dissipation.

IV. CIRCUIT DIAGRAM



SIMULATION RESULT **LAYOUT**





V. CONCLUSION

In this paper, a high voltage generator circuit with an on chip oscillator, a charge pump and a voltage regulator has been implemented and investigated. Measured results show that the presented charge pump system has better performance in efficiency (83.3%) and power dissipation (150.48 _W). The results show good accordance with the simulation and layout abstraction.

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