Analysis and Design of Modified Parity Generator and Parity Checker using Quantum Dot Cellular Automata

P.Ilanchezhian
Associate Professor, Department of IT, Sona College of Technology, Salem

Dr.R.M.S.Parvathi
Principal, Sengunthar College of Engineering, Tiruchengode,

Abstract- In preceding few years' further efforts has been done on error detection and error correction in digital transmission systems. This paper proposed the modified parity generator and parity checker circuits using QCA whose polarizations are improved and the output signal is found vigorous. QCA projected a new method to estimation in that arrangement of information at a circuit accomplished using electrons place in the quantum cell. As a result, the digital devices are more acceptable in noisy environment and they can perform more consistent. Finally, the functionality of the generator and checker is verified using QCA designer tool. The proposed design need only about 60% of the hardware compared to previous design with same clocking performance.

Keywords – Digital Circuits, Exclusive-OR gate, Parity generator and Parity Checker, Quantum dot cellular Automata.

I. INTRODUCTION

Digital communication systems are becoming progressively more striking because of the ever growing stipulate for data communication. Digital transmission offers data processing options and flexibilities not available with analog transmission. Normally digital circuits are less subject to distortion and intervention than are analog circuits. Because binary digital circuits operate in one of two states either fully on situation or fully off situation. Digital circuits are more reliable and can be produced at a low cost. Digital hardware is more flexible in implementation than analog hardware. Error correction technique is a most important area that has exploited for used in the communication systems [1]. Because of error detection and correction parity generator and checker circuit has being exploited in many applications such as Satellite communication, Compact disc players, broadband, Wireless communications, digital television, Wireless Sensor networks etc[2-3].

Nano technology based Quantum dot cellular automata (QCA) cell produce a new way to digital systems [4-14]. QCA is a computational methodology as an alternate to field effect transistor (FET) [15] devices. It is developed at the ATIPS Laboratory, at the University of Calgary, QCA Designer currently supports three different simulation engines, and many of the CAD features required for complex circuit design. [16-17]. In order to represent binary information logic 1 and logic 0 the cell polarization P = +1 and P= -1 is used respectively [15], [18]. QCA Inverters that use 45^0 and 90^0 cells orientations have been developed [19].The QCA majority gate has four terminal cells out of which three are representing input terminal cells and the remaining one represents the output cell [19-20]. The another type of majority gate consist of six terminals out of which five are representing input terminal cells and the remaining one represents the output cell [21]. Inverters that use 45^0 and 90^0 cells orientations have been developed [22]

II. EXCLUSIVE –OR

Exclusive –OR functions are very helpful in digital systems for error detection and error correction codes. Generally the exclusive –OR denoted by the symbol $\oplus$, is a logical operation that performs the following Boolean function,

$$A \oplus B = AB' + A'B \quad (1)$$

The Exclusive –OR is equal to one if only A is equal to one or if only B is equal to one, but not when both are

equal to one or when both are equal to zero. The majority gate implementation of Exclusive-OR [23] function is shown in Figure 1.

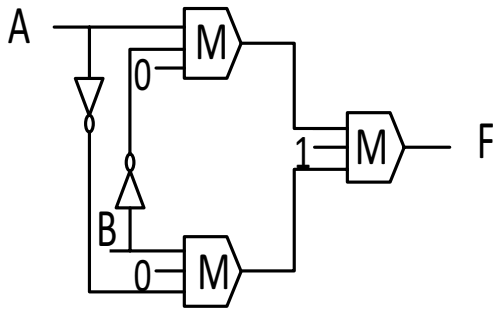

Figure 1. Majority gate implementation of Exclusive-OR gate

III. PARITY GENERATOR AND CHECKER

The parity generator and checker circuits are more important for digital data broadcast and reception. Generally, a parity bit is used for detecting errors during broadcast of binary information sequence. A parity bit is an additional bit inserted with binary information to make the number of one's either odd or even. The information message sequence including the additional bit is transmitted and then verified at the receiving point for errors. An error is detected if the verified additional bit does not correspond with the transmitted information. The digital circuit that creates the parity bit in the transmitter area is called a parity generator. The majority gate implementation of the parity generator circuit is shown in Figure 2.

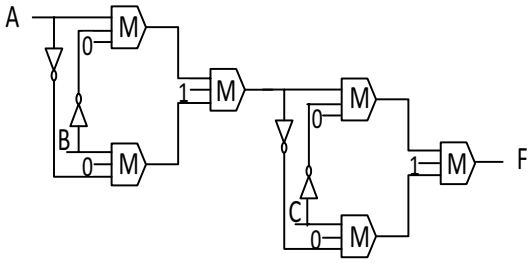

Figure 2. Majority gate implementation of Even Parity generator circuit

The digital circuit that verifies the additional bit in the receiver section is called a parity checker. The majority gate implementation of the parity checker is shown in Figure 3. Consider three bit information sequence to be transmitted together with an even parity bit. For even parity, the bit P must be generated to make the total number of one's even including additional bit. Here the additional bit constitutes an odd function because it is equal to one for those minterms whose numerical values have odd number of one's. The three bits in the information sequence together with the additional information are transmitted to their destination where they are applied to a parity verification circuit to verify the possible errors during broadcast. Since the information was transmitted with even parity the four bits received must have an even number of one's. An error occurs during the broadcast if the four bits received have an odd number one's indicating that one bit has changed in value during broadcast. The output of the parity checker denoted by F will be equal to one if an error occurs.

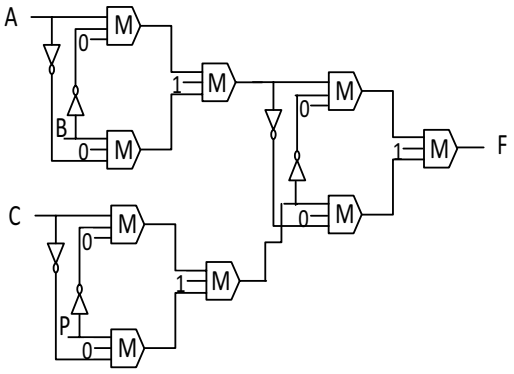

Figure 3. Majority gate implementation of Even Parity Checker circuit

Consider a general rule in a digital system where the transmission system is relatively short, it may be assumed that the probability of a single bit error is very small and that of a double bit error and higher order errors is extremely small. The parity error detection system cannot detect an any odd number of errors because such kind of errors will not destroy the parity of the transmitted group of bits. However, it detects any even number of errors. When several binary words are transmitted or received in succession, the resulting collection of bits can be regarded as a block of data, having rows and columns. In this the parity bits are assigned to both row and columns then the scheme is called block parity. It makes it possible to correct any single error occurring in data word and to detect any two errors in a word. One of the important error detection and error correcting code is hamming code. This code uses a number of parity bits dependent on the number of information bits located at certain positions in the code group. Generally, the hamming code can be constructed for single error correction. To perform these first find out the number of parity bit. Then find out the locations of the parity bits in the code and assigning values to parity bits. After that corresponding group of bits must be checked for proper parity. Once all parity checks, binary word is formed by resulting first bit as least significant bit. This word provides bit location where the error has occurred. If word has all bits 0 then there is no error in the hamming code.

IV. QCA IMPLEMENTATION

QCA computation proceeds by orientation of cells based on polarization of neighboring cells. The QCA inverter is built by neighboring QCA cells on the diagonal, which causes Coulomb forces to place the two electrons in opposing wells of the cell compared to the source. The quantum dot cellular automata implementation of parity generator circuit is shown in Figure 4. This circuit is designed with 6 majority gates and 4 invertors. The quantum dot cellular automata layout implementation of parity checker circuit is shown in Figure 5. This circuit is designed with 9 majority gates and 6 invertors. Similarly, all the computation of the generator and checker circuit is done with the help of Exclusive OR gate. It is designed with 3 majority gates and 2 invertors.

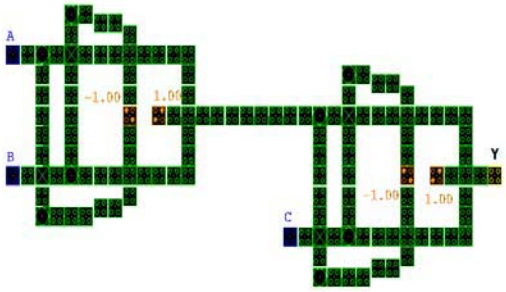

Figure 4. QCA implementation of Parity Generator

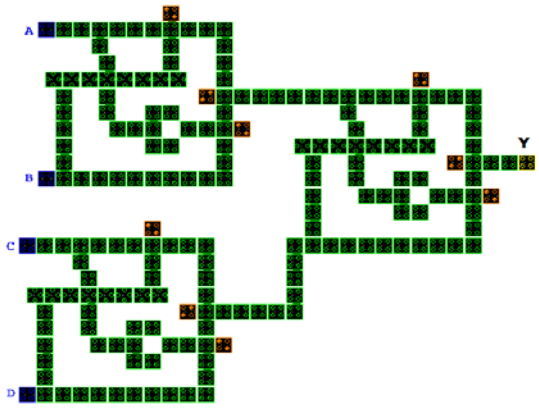

Figure 5. QCA implementation of Parity Checker

V. RESULTS

The proposed parity generator circuit and parity checker circuit are designed and simulated by using the Quantum dot Automata designer tool. Initially we generate the exclusive –OR function QCA layout and then we design the even parity generator and even parity checker layouts. To preserve reliability with size dimensions in previous publications [24], [19], we believe that the QCA cells are made of 2nm quantum dots. The cells are divided by 10nm. Thus, the area of the proposed parity generator is 682.62nm*291.59nm and the area of parity checker circuit is 602.13nm*487.69nm. The speed and clocking of the proposed design is comparable to the original design [24],[19]. Table I lists the area, speed and clocking of the proposed parity generator and checker along with those of the existing one [24], [19]. It is seen from Table I that the planned design requires only about 60% of the hardware compared to the existing one with the same speed and clocking performance. Thus, the simulation results are consistent with our theoretic results.

TABLE - I AREA OF PARITY GENERATOR AND CHECKER

Logical Structure	Previous Structure		New Structure		CLK
	Complexity	Area	Complexity	Area	
Exclusive-OR	87 cells	290nmX260nm	64 cells	234.04nmX224.37nm	simple
Parity generator	241 cells	935nmX625nm	135 cells	739.23nmX291.59nm	simple
Parity Checker	323 cells	812nmX595nm	197 cells	602.13nmX487.69nm	simple

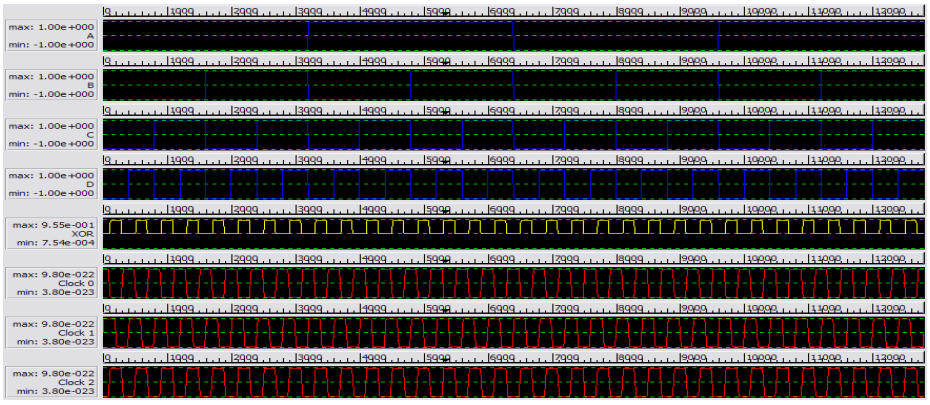

Figure 6 Simulation result of Parity Checker

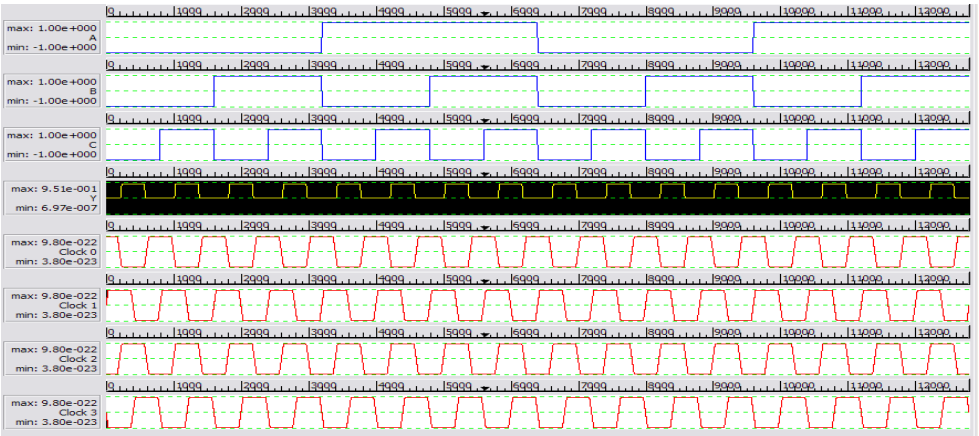

Figure 7 Simulation result of Parity Generator

The simulation result of Parity Generator and Parity Checker using QCA designer tool is shown in the Figure 6 and Figure 7 respectively. The function of even Parity Generator and Checker is verified based on Boolean function table.

VI. CONCLUSION

In this paper, a novel QCA even parity generator and even parity checker design has been presented that reduces the number of QCA cells in comparison to previously established designs. The proposed QCA even parity generator and even parity checker structure is based on a new algorithm that requires only three input majority gates and two inverters for QCA implementation of Exclusive-OR function. The projected QCA parity generator and checker has been design and simulated using the QCA Designer tool for the three-bit information case. The planned design requires only 60% of the hardware compared to the existing one with the same speed and clocking performance.

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