

# Designing Ripple Carry Adder using A new Design of the CMOS Full-Adders

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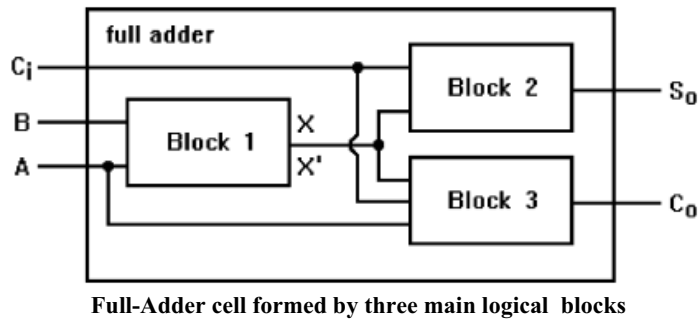
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**Abstract -** This paper presents a method to Designing Ripple Carry Adder using CMOS Full-Adders for Energy-Efficient Arithmetic Applications. We present two high-speed and low-power full-adder cells designed with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced power-delay product (PDP). We carried out a comparison against other full-adders reported as having a low PDP, in terms of speed, power consumption and area. All the full-adders were designed with a 0.18 $\mu$ m CMOS technology, and were tested using a comprehensive test bench that allowed to measure the current taken from the full-adder inputs, besides the current provided from the power-supply. Post-layout simulations show that the proposed full-adders outperform its counterparts exhibiting an average PDP advantage of 80%, with only 40% of relative area.

**Keywords:** Ripple Carry-Adder. Arithmetic, full-adder, high-speed, low-power.

## I. INTRODUCTION

Designing Ripple Carry Adder using CMOS Full-Adders is a technique that has been introduced to reduce the power consumption using a new cmos full-adder design. ENERGY-EFFICIENCY is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of very high-speed circuits. The power-delay product (PDP) metric relates the amount of energy spent during the realization of a determined task, and stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies, and scenarios. Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. As stated above, the PDP exhibited by the full-adder would affect the system's overall performance [1]. Thus, taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems. In this paper, we report the design and performance comparison of two full-adder cells implemented with an alternative internal logic structure, based on the multiplexing of the Boolean functions XOR /XNOR and AND / OR, to obtain balanced delays in SUM and CARRY outputs, respectively, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption. The resultant full-adders show to be more efficient on regards of power consumption and delay delay when compared with other ones reported previously as good candidates to build low-power arithmetic modules.

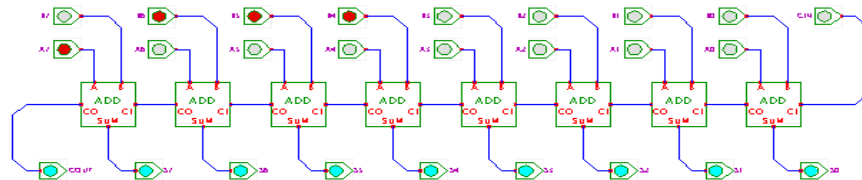


Full-Adder cell formed by three main logical blocks

## II . Designing Ripple Carry adder

### Circuit Description

A standard 8-bit **ripple-carry adder** built as a cascade from eight 1-bit full-adders. Click the input switches or use the following bind keys : ('c') for carry-in, ('a','s', ..., 'k') for A0..A7 and ('1','2', ..., '8') for B0..B7. To demonstrate the typical behavior of the ripple-carry adder, very large gate-delays are used for the gates inside the 1-bit adders - resulting in an addition time of about 0.6 seconds per adder. Note that each stage of the adder has to wait until the previous stage has calculated and propagates its carry output signal. Obviously, the longest delay results for operands like A = 0b0000000, B=0b1111111 or A=0b01010101 and B=0b10101010 (select these, and then switch carry-in to both 0 and 1, and watch the circuit to settle). Therefore, the total delay of a ripple-carry adder is proportional to the number of bits. Faster adders are often required for bit widths of 16 or greater. Each full-adder built by using a new CMOS technology which consumes less power. The power-delay product (PDP) metric relates the amount of energy spent during the realization of a determined task, and stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies, and scenarios. The PDP exhibited by the full-adder would affect the system's overall performance [1]. Thus, taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems.



8-Bit Ripple Carry – Adder using Full - Adders

## III. PREVIOUS FULL -ADDER OPTIMIZATIONS

Many papers have been published regarding the optimization of low-power full-adders, trying different options for the logic style (standard CMOS [2], differential cascode voltage switch (DCVS) [3], complementary pass-transistor logic (CPL) [4], double pass-transistor logic (DPL) [5], swing restored CPL (SR-CPL) [6], and hybrid styles [7]–[9]), and the logic structure used to build the adder module [10], [11]. The internal logic structure shown in Fig. 1 [12] has been adopted as the standard configuration in most of the enhancements developed for the 1-bit full-adder module. In this configuration, the adder module is formed by three main logical blocks: a XOR - XNOR gate to obtain  $S_o$  and  $C_o$  (Block 1), and XOR blocks or multiplexers to obtain the SUM ( $S_o$ ) and CARRY ( $C_o$ ) outputs (Blocks 2 and 3). A deep comparative study to determine the best implementation for Block 1 was presented in [13], and an important conclusion was pointed out in that work: the major problem regarding the propagation delay for a full-adder built with the logic structure shown in Fig. 1, is that it is necessary to obtain an intermediate signal and its complement, which are then used to drive other blocks to generate the final outputs. Thus, the overall propagation delay and, in most of the cases, the power consumption of the full-adder depend on the delay and voltage swing of the  $C$  signal and its complement generated within the cell. So, to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of intermediate signals to control the selection or transmission of other signals located on the critical path. Examining the full-adder's true-table in Table I, it can be seen that the  $S_o$  output is equal to the A X-OR B value when  $C=0$ , and it is equal to complement of A X-OR B when  $C=1$ . Thus, a multiplexer can be used to obtain the respective value taking the  $C$  input as the selection signal. Following the same criteria, the  $C_o$  output is equal to the A.B value when  $C=0$ , and it is equal to A+B value when  $C=1$ . A gain,  $C$  can be used to select the respective value for the required condition, driving a multiplexer.

TABLE I TRUE -TABLE FOR A 1-BIT FULL -ADDER :A,B, AND C ARE INPUTS ;  $S_o$  AND  $C_o$  ARE OUTPUTS

C	B	A	$S_o$	$C_o$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the A x-or B and complement of A x-or B signals, another block to obtain the A.B and A+B signals, and two multiplexers being driven by the  $C$  input to generate the  $S_o$  and  $C_o$  outputs, as shown in Fig. 2 [13].

*The features and advantages of this logic structure are as follows:*

- There are not signals generated internally that control the selection of the output multiplexers. Instead, the  $C$  input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.
- The capacitive load for the  $C$  input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the  $C$  signal falls on the critical path can be reduced.
- The propagation delay for the  $S_o$  and  $C_o$  outputs can be tuned up individually by adjusting the XOR / XNOR and the AND / OR gates; this feature is advantageous for applications where the skew between

arriving signals is critical for a proper operation (e.g., wave - pipelining), and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.

- The inclusion of buffers at the full-adder outputs can be implemented by interchanging the XOR / XNOR signals, and the AND / OR gates to NAND / NOR gates at the input of the multiplexers, improving in this way the performance for load-sensitive applications. Based on the results obtained in [13], two new full-adders have been designed using the logic styles DPL and SR-CPL, and the new logic structure presented in Fig. 2. Fig. 3 presents a full-adder designed using a DPL logic style to build the XOR / XNOR gates, and a pass-transistor based multiplexer to obtain the  $S_o$  output. In Fig. 4, the SR-CPL logic style was used to build these XOR / XNOR gates. In both cases, the AND / OR gates have been built using a powerless and groundless pass-transistor configuration, respectively, and a pass-transistor based multiplexer to get the  $C_o$  output.

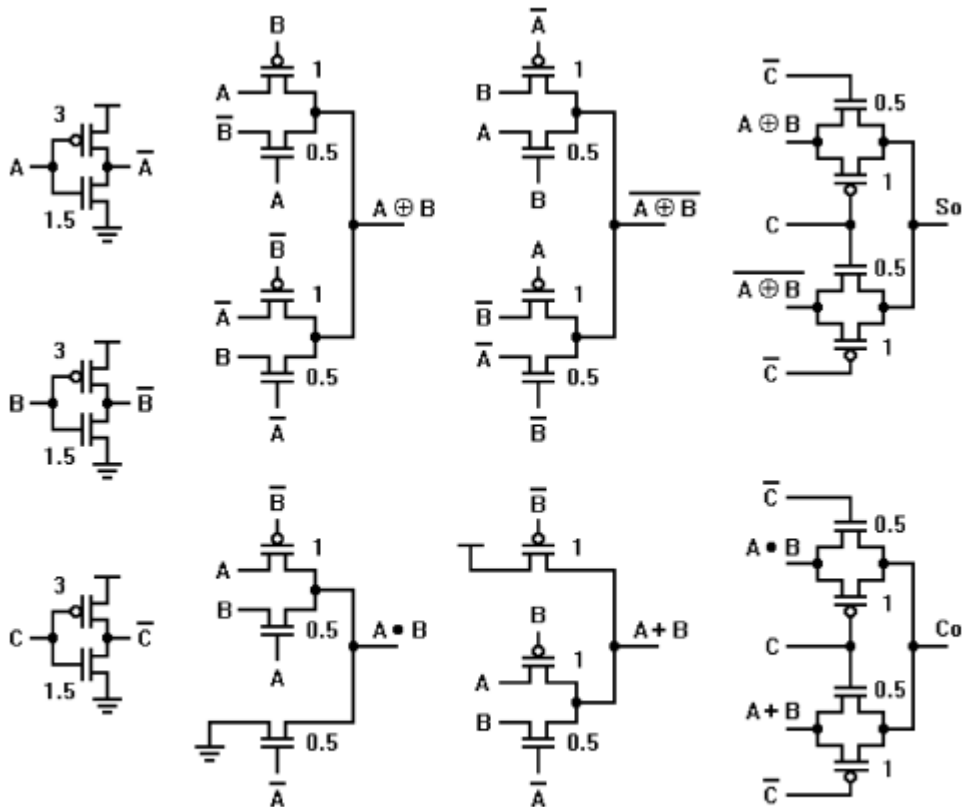


Fig. 3. Full-adder designed with the proposed logic structure and a DPL logic style (Ours1).

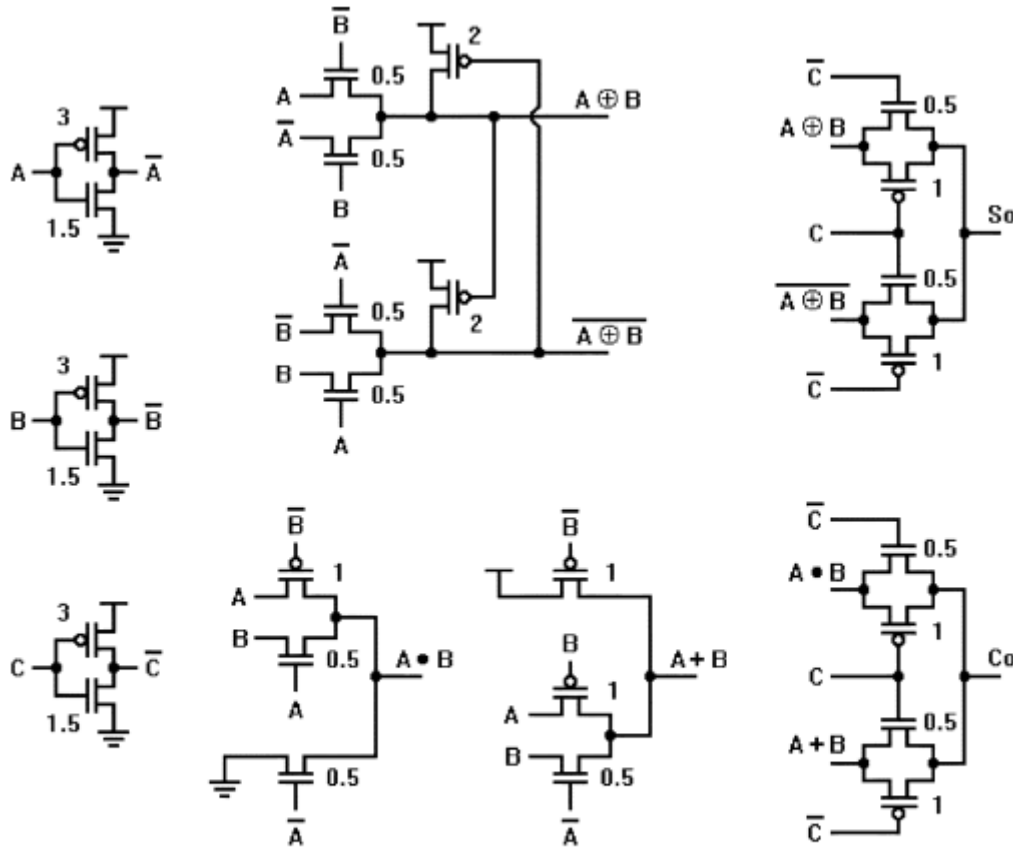


Fig. 4. Full-adder designed with the proposed logic structure and a SR-CPL logic style (Ours2).

#### IV. SIMULATION ENVIRONMENT

Fig. 5 shows the test bed used for the performance analysis of the full-adders. This simulation environment has been used for comparing the full-adders analyzed in [9], [14], with the addition of the inverters at the outputs. The size of the input buffers lets to experience some degradation in the input signals, and the size of the output buffers equals the load of four small inverters for this technology. This test bed is presented as a generalization of static CMOS gates driving and been drive n for the full-adder cell under test. The main advantage of using this simulation environment is that the following power components are taken into account, in addition to the dynamic one.

- The short-circuit consumption of the inverters connected to the device under test (DUT) inputs. This power consumption varies according to the capacitive load that the DUT offers at the inputs. Furthermore, the energy required to charge and discharge the DUT internal nodes when the module has no direct power supply connections (as for the case of pass-transistor logic styles), comes through these inverters connected at the DUT inputs.
- The short-circuit consumption of the DUT by itself, as it is receiving signals with finite slopes coming from the buffers connected at the inputs, instead of ideal ones coming from voltage sources.
- The short-circuit and static consumption of the inverters connected to the outputs of the DUT, which are due to the finite slopes and degraded voltage swing of the full-adder output signals.

TABLE II (SIMULATION RESULTS OF FULL ADDERS COMPARED (POWER IN  $\mu$ W, DELAY IN PS, PDP IN  $\mu$ W.NS, AREA IN  $\mu$ M<sup>2</sup>, FREQUENCY IN GHZ AND VDD IN V)

scheme		avg pwr	pwr supply	dynamic	static	short-circuit	% add/top	delay	PDP	area	F max	Vdd min
new14T	top	457.7	457.7	256.3	2.7	198.7	64.2	372	109.3	257	0.25	1.2
	fa	293.8	101.2	145.8	2.7	145.3						
hpsc	top	456.1	456.1	314.4	0.0	141.7	63.9	425	123.8	412	0.25	1.2
	fa	291.3	169.0	186.7	0.0	104.7						
hybrid	top	391.7	391.7	321.1	0.0	70.6	60.9	287	68.5	459	0.80	0.7
	fa	238.7	124.2	204.1	0.0	34.6						
hybrid_cmos	top	370.1	370.1	280.1	0.0	90.0	60.9	325	73.3	427	0.80	0.8
	fa	225.5	176.8	177.5	0.0	48.0						
cpl	top	266.1	266.1	183.6	0.2	82.3	54.6	284	41.3	378	1.50	0.6
	fa	145.3	135.7	103.7	0.2	41.4						
Ours1	top	184.8	184.8	109.2	0.0	75.6	29.8	289	15.9	246	1.25	0.6
	fa	55.1	34.7	53.8	0.0	1.3						
Ours2	top	190.4	190.4	116.6	0.0	73.8	31.8	278	16.8	243	1.25	0.6
	fa	60.6	48.4	54.5	0.0	6.1						

V. SIMULATION RESULTS

We compared the performance of 7 full-adders, named: new14T [15], hpsc [7], hybrid [8], hybrid\_cmos [9], cpl [10], Ours1 and Ours2. The schematics and layouts were designed using a TSMC 0.18- m CMOS technology, and simulated using the BSIM3v3 model (level 49) and the post-layout extracted netlists containing R and C parasitics. Simulations were carried out using Nanosim [16] to determine the power consumption features of the designed full-adders, and Hspice [17] to measure the propagation delay for the output signals. In order to have a fair comparison, we took the transistors sizes for each full-adder that were reported in the correspondent paper, and made all the layouts with a homogeneous arrangement.

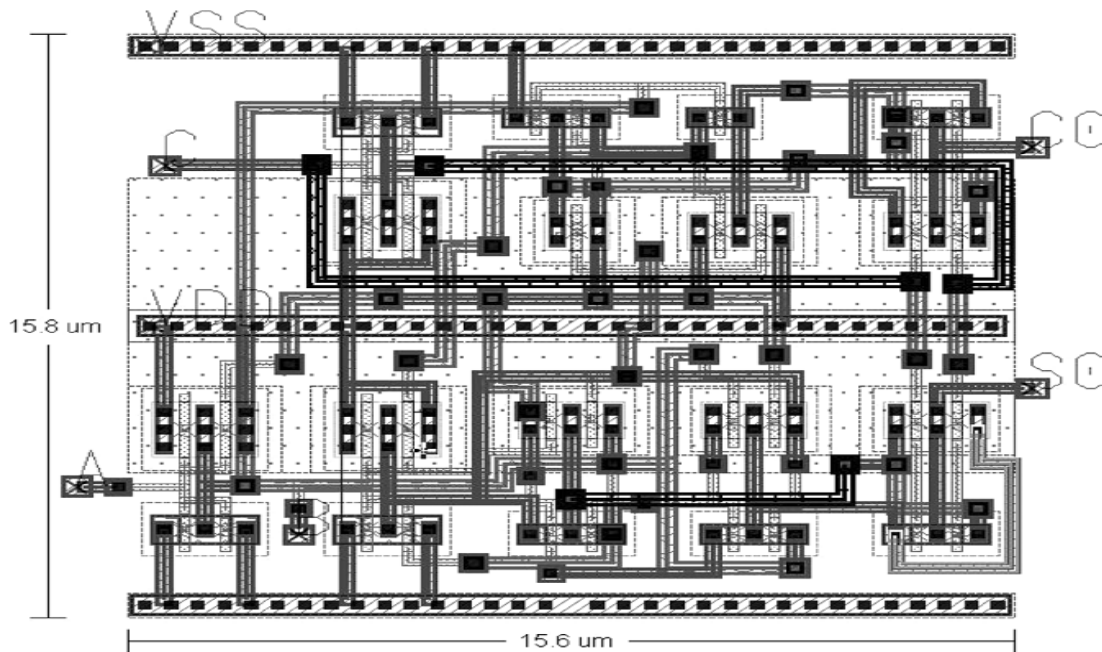


Fig 6: Layout of the Proposed Full-Adder Ours 1

Table II shows the simulation results for full-adders performance comparison, regarding power consumption, propagation delay, and PDP. All the full-adders were supplied with 1.8 V and the maximum frequency for the inputs was 200 MHz. This table reports the results for the whole test bed (top) and for the full-adder alone (add). It is worth to observe that in some cases, the power consumed from the power-supply (pwr supply) for the full-adder is smaller than the total average power (avg power). This is because of, for some logic styles (e.g., pass-transistor style), some current is taken from the inputs of the full-adder and is used to charge the internal nodes. As mentioned above, it is the importance of considering the power consumption of the input buffers in the top test-bed. From the results in Table II, we can state the following.

- Only two full-adders exhibit static-dissipation. These are the new14T and cpl adders, which are implemented with logic styles that have an incomplete voltage swing in some internal nodes, causing this consumption component.
- The power consumption improvements of the full-adders taken in descending order correlate with the optimizations reported in the cells have been shown to perform worse than other ones when considering the power consumption of the whole test-bed.
- On regards of the implementation area obtained from the layouts, it can be seen that the proposed full-adders require the smallest area (up to 40% of relative area), which can also be considered as one of the factors for presenting lower delay and power consumption, as it implies smaller parasitic capacitances being driven inside the full-adder.

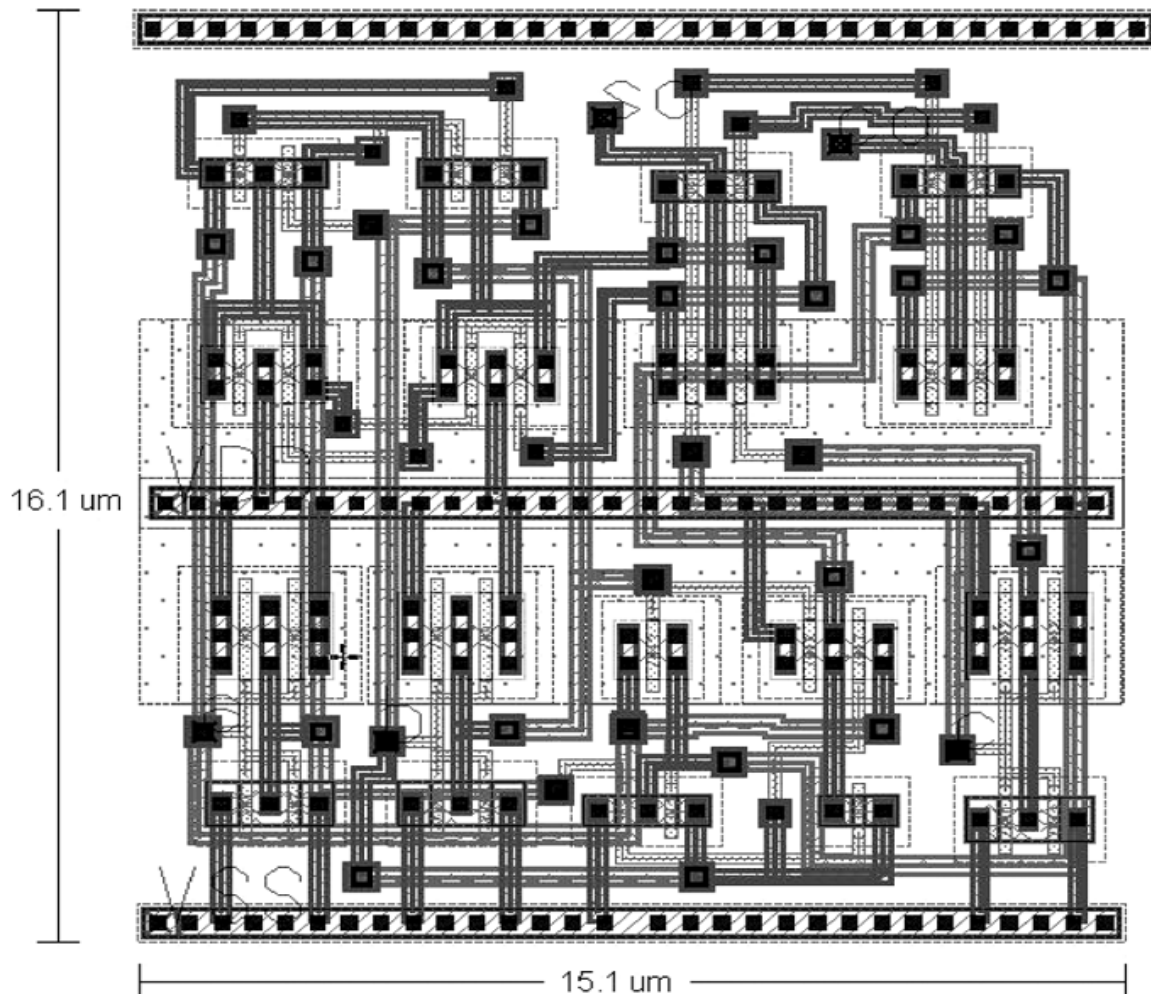


Fig 7: Layout of the Proposed Full-Adder Ours 2

The reason for the smaller area, compared to other full-adders that have less transistors, is that the size of the transistors in the proposed full-adders is minimal and not larger than  $2\ \mu\text{m}$  (except for the symmetrical response inverters at the inputs), while for other full-adders the transistor sizes are in the range of  $4$  to  $6\ \mu\text{m}$ . Figs. 6 and 7 show the layouts of the proposed full-adders, with the correspondent side by side dimensions.

• Finally, we determined the maximum frequency that each full-adder can operate, while being supplied with  $1.8\ \text{V}$ . The proposed full-adders reach up to  $1.25\ \text{GHz}$ , only surpassed by cpl cell, at the expense of major power consumption and area. The reason for running the power-delay performance simulations at  $200\ \text{MHz}$  was due to the full adders that work only up to  $250\ \text{MHz}$ .

## VI. CONCLUSIONS

An alternative internal logic structure for designing full-adder cells was introduced. In order to demonstrate its advantages, two full-adders were built in combination with pass-transistor powerless/groundless logic styles. They were designed with a TSMC  $0.18\text{-}\mu\text{m}$  CMOS technology, and were simulated and compared against other energy-efficient full-adders reported recently. Hspice and Nanosim simulations showed power savings up to  $80\%$ , and speed improvements up to  $25\%$ , for a joint optimization of  $85\%$  for the PDP. The area utilization for the proposed full-adders is only  $40\%$  of the largest full-adder compared, and the power-supply voltage for the proposed full-adders can be lowered down to  $0.6\ \text{V}$ , maintaining proper functionality

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