Comparision between 3 Pulse 7 Level And 12 Pulse 7 Level Multilevel Inverter

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Abstract—This paper analyses the structure of new type of multilevel inverters suitable for high voltage and high power applications. The proposed topologies significantly reduces the number of dc voltage sources, switches, IGBTs, and power diodes as the number of output voltage levels increases. Two type of multilevel inverters have been compared in this paper. The objective of this paper is to understand the working and simulation study of 3 pulse 7 level and 12 pulse 7 level multilevel inverter by PWM technique using MATLAB/SIMULINK software.

Keywords—Multipulse converters, Voltage source converters, Multilevel inverters, FACTS devices.

I. INTRODUCTION

The voltage source inverters produce a voltage or a current with levels either 0 or ±V dc they are known as two level inverters. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high switching frequency along with various Pulse Width Modulation (PWM) strategies. In high power and high voltage applications, these two level inverters, however, have some limitations in operating at high frequency. It may be easier to produce a high power, high voltage inverter with the multi-level structure because of the way in which device voltage stresses are controlled in the structure. Increasing the number of voltage levels in the inverters without requiring higher ratings on the individual devices can increase the power rating.

The unique structure of Multi-level voltages sources inverters allow them to reach high voltages with low harmonics without the use of transformer or series connected synchronized switching devices. As the number of voltage levels increases, the harmonic content of output voltage waveform decreases significantly. The capability of proposed structure in producing all odd and even output voltage levels is proved by simulation result for a 3 pulse 7 level multilevel inverter and a 12 pulse 7 level multilevel inverter.

II. MULTILEVEL INVERTER

An inverter is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high-voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries.

III. INVERTER TOPOLOGIES

The general structure of multi-level converter is to synthesize a near sinusoidal voltage from several levels of dc voltages, typically from capacitor voltage sources. As number of levels increases, the synthesized output waveform has more steps, which provides a staircase wave that approaches a desired waveform. Also, as steps are added to waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of voltage levels increases. This increases the power quality.

Numerous methods have been investigated to increase the number of levels in the multi-level inverter's output. Multilevel voltage source inverter is recognized as an important alternative to the normal two level voltage

source inverter especially in high voltage application. Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved.
It exhibits several attractive features such as simple circuit layout, less components counts and modular in structure. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. In this paper, a 3 pulse 7 level multilevel inverter and a 12 pulse 7 level multilevel inverter employ a new technique to obtain a multilevel output using less number of power semiconductor switches when compared to ordinary cascaded multilevel inverter.
The comparisons between the topologies that have been made in this paper are as follows

- 3 pulse 7 level multilevel inverter
- 12 pulse 7 level multilevel inverter

1) 3 Pulse 7 Level Multilevel Inverter

The 3 Pulse 7 Level Multilevel Inverter consists of less number of switches when compared to the other familiar topologies. The initial cost reduces because of the switch reduction. So, it looks attractive and an apt one for industrial applications.

The general circuit diagram of the proposed multilevel inverter is shown in the fig.1. The switches are arranged in the manner as shown in the figure. For this topology, we just need to add only one switch for every increase in levels, so initial cost gets reduced. Let us see operation in the next subdivision in detailfor the 3 Pulse 7 Level inverter as shown in fig.1.

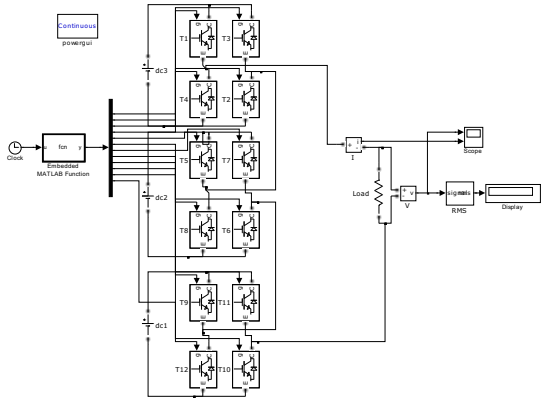


Fig.1 MATLAB/Simulink circuit for 3 Pulse 7 Level inverter.

Simulation results are shown here by the help of MATLAB/Simulink for 3 Pulse 7 Level inverter in fig 1.The results are shown by PWM control technique. The batteryof 25 volts DC each is chosen for input supply. The load connected here is the same R load. The IGBTs are used in this topology forhigher stability of the circuit. DC voltages are compared with different types of triangular waves to obtain the gate pulses. The relational operators areused. The pulse width of the pulses required determines thevalue of the constants. Pulse width is determined by the ontime of each switch and these signals are used for switchingthe IGBT's. Theoutputs from the comparison operational amplifiers arecompared and given toAND gate for obtaining the PWMpulses[1,2]. These signals areused as the gating signals for the switches.
The below tableshows the various different switching states in this proposed topology.

S.NO	ConductingSwitches	OutputVoltag
1	S1,S3,S5,S7,S9,S11	$+V_{DC}$
2	S1,S3,S5,S6,S9,S11	$+2V_{DC}$
3	S3,S4,S7,S8,S9,S10	$+3V_{DC}$
4	S1,S3,S7,S8,S9,S10	$+4V_{DC}$
5	S1,S2,S7,S8,S9,S10	$+5V_{DC}$
6	S3,S4,S5,S7,S9,S10	$+6V_{DC}$
7	S1,S3,S5,S7,S9,S10	$+7V_{DC}$
8	S1,S2,S5,S7,S9,S10	$+8V_{DC}$
9	S3,S4,S5,S6,S9,S10	$+9V_{DC}$
1	S1,S3,S5,S6,S9,S10	$+10V_{DC}$
1	S1,S2,S5,S6,S9,S10	0
1	S1,S3,S5,S6,S9,S10	$-V_{DC}$
1	S3,S4,S5,S6,S9,S10	$-2V_{DC}$
1	S1,S2,S5,S7,S9,S10	$-3V_{DC}$
1	S1,S3,S5,S7,S9,S10	$-4V_{DC}$
1	S3,S4,S5,S7,S9,S10	$-5V_{DC}$
1	S1,S3,S7,S8,S9,S10	$-6V_{DC}$
1	S3,S4,S7,S8,S9,S10	$-7V_{DC}$
1	S1,S3,S5,S6,S9,S11	$-8V_{DC}$
2	S1,S3,S5,S6,S9,S11	$-9V_{DC}$
2	S1,S3,S5,S6,S9,S11	$-10V_{DC}$

Table I
Switching states

Values of VDC for different switching states are as shown in Table I. The firing pulses are obtained from the embedded Matlab function. These pulses are given to 3 Pulse 7 Level inverter.

2) 12 pulse 7 level multilevel inverter

Numerous methods have been investigated to increase the number of levels in the multilevel inverter's output. Strong efforts have been made in order to reach minimum harmonic distortion in the VSI's output voltage. A strategy to build an 12 pulse 7 level equivalent output voltage waveform, which employs a twelve-pulse along with an seven-level inverter is presented in [4] this paper.

The 12 pulse 7 level multilevel inverter operation is assembled by connecting two identical three-phase bridges to three-phase transformers in a parallel VSC configuration. Each branch in the six-pulse converter must have a displacement of 120° among them. The upper switch is conducting while the lower one is open and vice versa (180° voltage source operation) [3]. A 30° displacement in the firing sequence of both converters should be considered. This produces the output pulses and the levels required to generated output waveform.

The 3 phase transmission line is the source and the 12 pulse and 7 level voltage waveform with improved power quality and less Total Harmonic Distortion (THD) is the output voltage.

The MATLAB/Simulink circuit for 12 Pulse 7 Level inverter is shown in fig. 2.

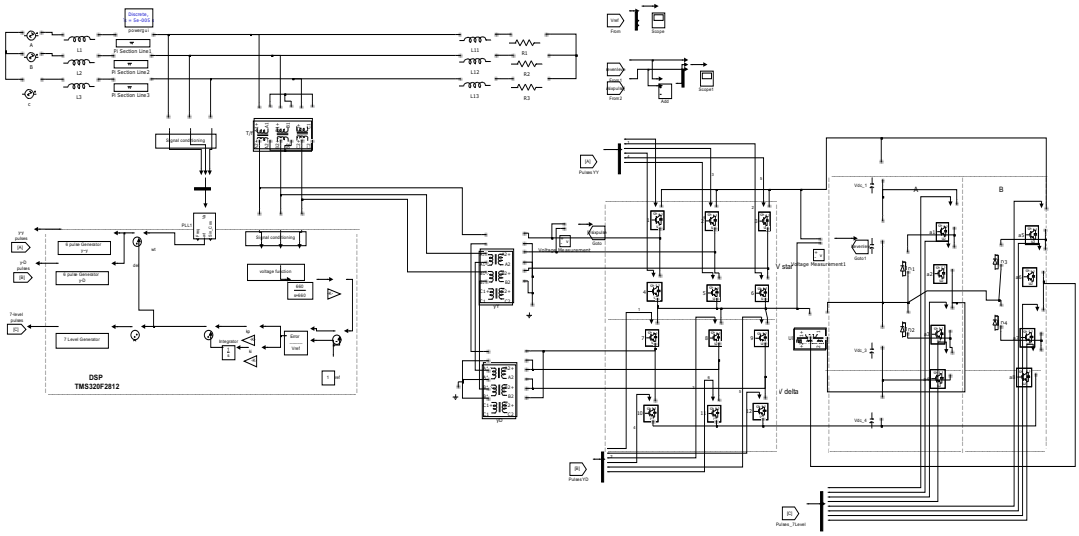


Fig.2 MATLAB/Simulink circuit for 12 Pulse 7 Level inverter

The Total Harmonic Distortion (THD), which is defined by

$$THD_{VU} = \sqrt{\frac{\sum_{n=2}^{n} V_{Un}^2}{V_{U1}^2}}$$

MATLAB for a value n = 7200, with increments of a = 0.0001. With these parameters, the minimum THD becomes 2.358% with a = 0.5609 , value employed in previous figures. According to the IEEE Std. 519, the distortion limits indicate that the allowed THD voltage is 10% in dedicated systems, 5% in general systems, and 3% for special applications as hospitals and airports [5].

2.1 Phase-Locked-Loop (PLL)

The Synchronizing Circuit is responsible for determining the system frequency and the phase-angle of the controlled AC bus fundamental positive sequence voltage [6]. The Phase-Locked-Loop (PLL) utilizes the Stationary Reference Frame in order to reduce the computational cost, and helps to improve the system's dynamic performance [7]. The digital PLL is an algorithm able to detect the phase of the fundamental voltage, through the synchronization of the output signal to the frequency and phase of the input one, without requiring a zero crossing subroutine at the input voltage, or to generate an internal reference signal for the input current [8]. The proposed strategy employs a tan function added to a correction value determined by the signs α and β,Fig. 3

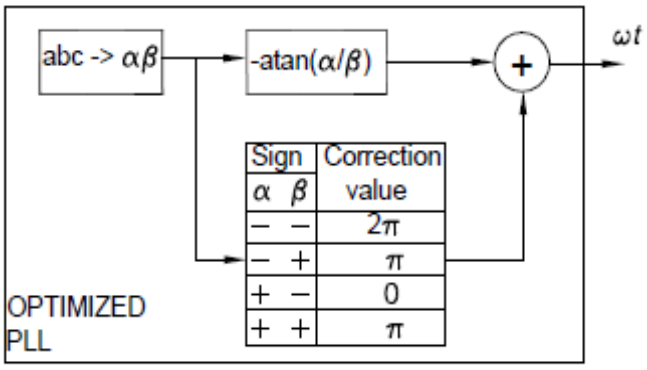


Fig. 3 Optimized PLL scheme.

2.2 Six-Pulse Generator

The second block is the six-pulse generator, responsible for generating the pulse sequence to fire the three-phase

IGBT array. It consists of an array of six-pulse spaced 60° each other. The IGBT will operate at full 180° for the *on* period and 180° for the *off* period. Any disturbance on the frequency will be captured by the synchronizing block, preventing malfunctioning. The falling border in the synchronizing block output signal is added to a series of six 60° spaced signals. The modulus operator with the two argument gives the needed *on* sequence that will be sent to the gate opto-coupler block,which will feed each six- pulse converter. The *off* sequence turns out on a similar way but waiting 180° to keep the same *on* and *off* duration in each IGBT.

2.3 Seven-Level Pulse Generator

To operate the seven-level inverter, six times the frequency of the six-pulse generator must be ensured. This is achieved by monitoring the falling border in the novel PLL output signal, using it along with the modulus operator with the $/3$
argument. This signal will be the period for the seven-level generator which will change its state each $/42$ rad.

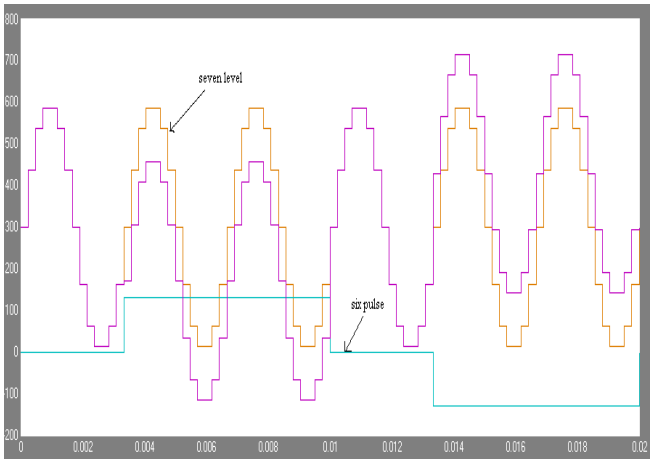
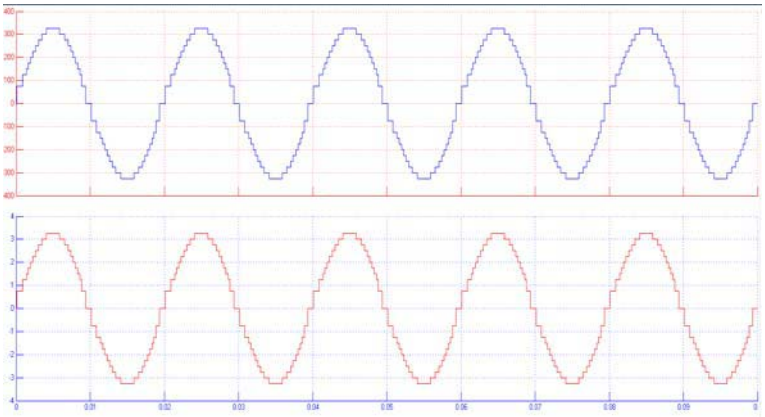


Fig. 4 Mixing seven-level, six-pulse signals

IV. SIMULATION RESULTS

To examine the performance of 3 pulse 7 level and 12 pulse 7 level multilevel inverter in generation of a desired output voltage waveform it is simulated in MATLAB- SIMULINK environment. This inverters can generate staircase output voltage waveform. Table I shows the switching pattern of structure in Fig. 1 to produce different output voltage levels for 3 pulse 7 level multilevel inverter. Fig. 2 shows the control block diagram of 12 pulse 7 level multilevel inverter.



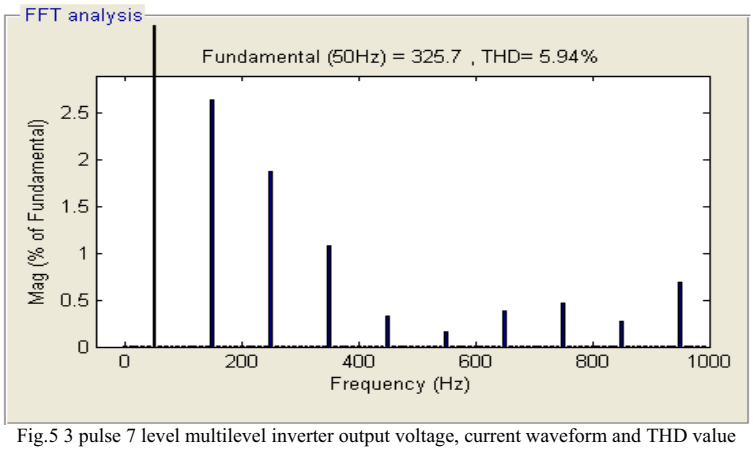
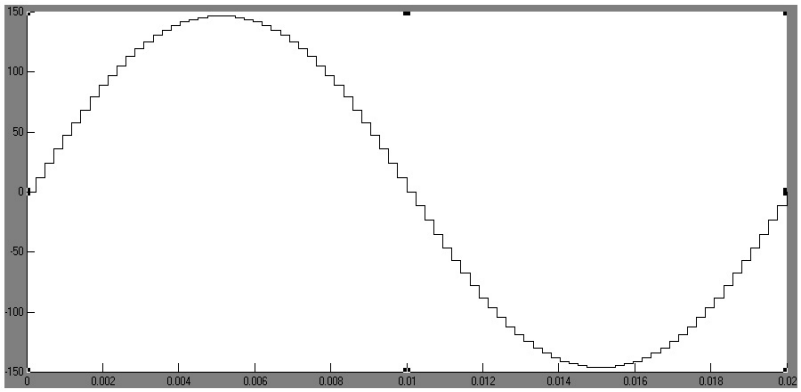


Fig.5 3 pulse 7 level multilevel inverter output voltage, current waveform and THD value



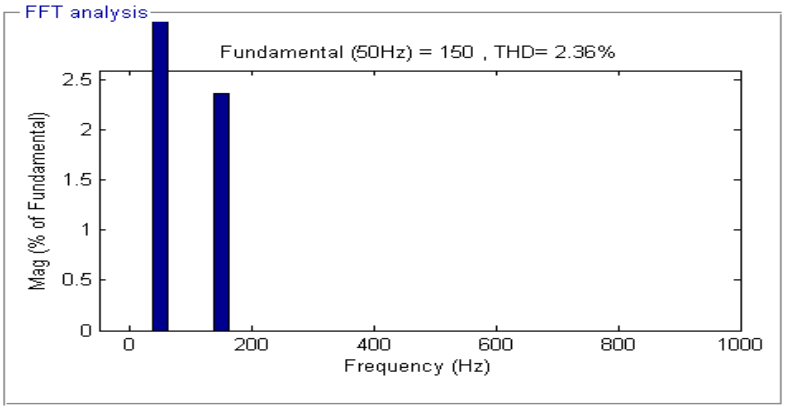


Fig.6 12 pulse 7 level multilevel inverter output voltage and THD value

The main idea in control strategy is to deliver the load a voltage that minimizes the total harmonic distortion with respect to reference voltage.The simulation results for a 3 pulse 7 level multilevel inverter and a 12 pulse 7 level multilevel inverter is shown in the fig. 5 and fig 6 respectively

V. CONCLUSION

Thesimulation of 3 pulse 7 level and 12 pulse 7 level multilevel inverter by PWM technique using MATLAB/SIMULINK softwareis successfully done. Acomparison betweenthe 3 pulse 7 level multilevel inverter and 12 pulse 7 level multilevel inverter topology isshowninTableIIwhichclearly shows thepercentagereductioninthe Total Harmonic Distortion.

INVERTER	THD (%)
3 pulse 7 level	5.94
12 pulse 7 level	2.36

Table II Total Harmonic Distortion.

The results of the simulation the 3 pulse 7 level multilevel inverter and 12 pulse 7 level multilevel inverter demonstrate that the later configuration has prominent feature compared to other multilevel inverters.The exhibited low THD, permits the system to be used in especial applications suitable for high voltage and high power applications. The 12 pulse 7 level multilevel inverter has ability to synthesize waveforms with better harmonics spectrum.The output waveform of multilevel inverter follows the sinusoidal waveform hence the harmonic contents are less. The power loss in the circuit is less due to less number of switches.

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