Analysis and characterization of VCO for UWB Application

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Abstract— In recent years, the design of voltage controlled oscillators has become the subject of extensive research. Due to increasing demands for reconfigurable communication systems such as the software defined radio (SDR), new wideband VCO architectures are required.
This paper presents a wideband voltage controlled oscillator topology based on an active inductor generating negative resistance. The proposed architecture covers a frequency band between 5.47 GHz to 6.62GHz with phase noise of -113.7 dBc/Hz at 1 MHz offset from the 5.7GHz carrier frequency. Power consumption of the oscillator core is 3.068 mW from a 1.2 V supply. The circuit has been simulated in Cadence using UMC 0.18 µm CMOS model libraries.
Index Terms— UWB - CMOS – LCVCO- Phase Noise- Spiral Inductor

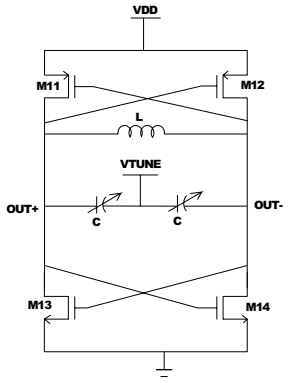
I. INTRODUCTION

1.1 INTRODUCTION TO UWB:

UWB technology has received significant interests to achieve high data rate communication. The Federal Communication Commission (FCC) has then released the 3.1-10.6GHz frequency band for the unlicensed usage of UWB devices.
An Ultra- Wide Band radio signal is one whose fractional band width (i. e. 3dB-band width divided by the center frequency) is large , typically 20%, where a few nanoseconds pulse generates a signal that is spread across a wide spectrum in frequency domain. On the other hand, an UWB radiator must not exceed electric field strength of 500 µV/m at 3 meter from the radiator in every 1MHz band. An UWB Transceivers have a built-in voltage Controlled oscillator, to generate a signal with the desired frequency (ωo rad/sec) used for up and down conversion. Wireless communication standards specify the minimum level of the received signal, the acceptable value of signal to noise ratio, the channel bandwidth, and the spacing between two adjacent channel, and power dissipation.
Therefore, the maximum value of permitted noise on the VCO and the minimum amount of power dissipation are a great challenge for the designer of UWB application.

1.2 INTRODUCTION TO VCO:

An oscillator is a system which generates a periodic output signal. The VCO are oscillators in which the output frequency is proportional to an applied external voltage. Thus, VCOs are found in telecommunication systems. Oscillators must have some sort of self-sustaining mechanism to ensure that they continue to generate these periodic signals for an indefinite period of time.
VCO can be classified into three topologies, ring topology, relaxation topology, and the harmonics one as shown in Figure 1-2. In a relaxation oscillator, the oscillation relies on nonlinear switching that charges and discharges a capacitor with a time constant. The oscillation frequency is tuned by varying this time constant. It is usually limited to moderate frequencies. Ring oscillators are normally designed by cascading an odd number of inverters in a loop. A variable resistor or current source is used for tuning. The frequency range can also be adjusted by digitally adding or removing inverters from the chain (coarse tuning). Although Ring and relaxation oscillators have advantages, such as highly integrated in VLSI, low power, small die area occupancy, and wide tuning range, it suffer from a poor frequency stability, which cause a higher noise. On the other hand, harmonic oscillator has an outstanding noise and jitter performance at high frequency. However, it suffers from its inherently narrow tuning range, and the integration of LC-based is more costly due to the large space allocated to on-chip inductors.
One of major applications for VCO is a frequency synthesizer, which provides sinusoidal/pulse signals at predetermined frequencies that is precisely controllable by digital words.



1.3 Why CMOS VCO:

Frequently, VCO circuits have been implemented in technologies such as bipolar or BiCMOS due to their high speed and low noise characteristics. However, these technologies are expensive, and are not area efficient. Moreover, they are not suitable for system-on-chip (SoC) integration and system in a –package (SiP). On the other hand, advantage of CMOS technology includes low power, higher manufacturing yield, and higher level of integration, with probability of integrating analog and digital circuits (mixed analog digital) on the same chip Figure. 3 shows the parallel LC tank circuit. The signal energy stored in the tank, Where C is the capacitance, L is the inductance; R is the parallel resistance, G is the equivalent transconductance of the tank and –G is the negative transconductance of the differential pair (energy restorer).

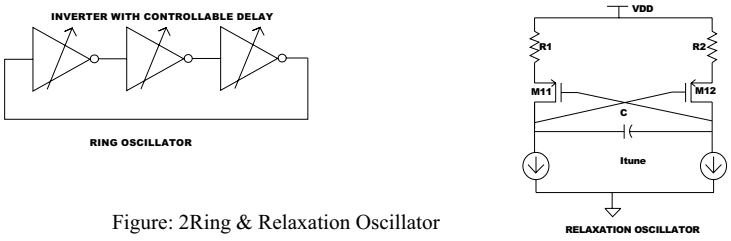


Figure: 2Ring & Relaxation Oscillator

LC-oscillator normally consists of two parts

1. An LC-tank responsible for the oscillation frequency
2. An active part which acts as a compensation n/w for the losses in the tank.

Oscillations can occur when:

i) The negative conductance of the active network cancels out the positive conductance (Loss) of the tank

ii) The closed loop gain has zero phase shifts.

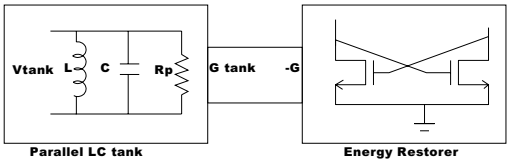


Figure: 3Parallel LC tank

1.4 IDEAL VCO SPECIFICATION

1) Low power
2) Wide tuning range
3) Small die area occupancy
4) High frequency (GHz)
5) Low noise

Assuming ideal varactors and MOSFETs is given by $\omega 0 = (1/2\pi\sqrt{LC})$
It can also be shown, under the same set of assumptions that the gm of each MOSFET must be
$g_m \geq RC/L$
for oscillation occur. For UWB application the harmonic oscillation is preferred in terms of phase noise harmonics concept and current consumption

II. CIRCUIT DESIGN

2. 1. An integrated inductor

The on-chip spiral inductor suffers from an even lower Q, due to eddy currents in the substrate and metal resistive loss. The most common structures of the on chip inductor are square, octagonal, and circular. The Main design parameters of a spiral inductor are its inductance L (ω), quality factor Q(ω) and self-resonance frequency fSR, which depends on the geometry of the spiral inductor. The quality factor QL of the inductor is given by:

$$Q = \omega L / R$$

Where ω is the oscillation frequency [rad/s]
L is the value of the inductance [H]
R is inductor's equivalent series resistance [Ω].
QL in practical silicon RF IC processes ranges from 5 to 10 and values of on-chip inductances range from 0.1 nH to 10 mH in practical RF IC processes. It can be shown that the oscillation frequency is given by:

$$\omega = 1/\sqrt{LC}$$

Tuning range TR can be calculated as the will known relation:
$Tr = 2(f_{max} -)/(f_{max} + fmin)$
Where f_{max} and $fmin$ are the maximum and minimum frequency respectively.

2.2 A MOS varactor

Varactor is a principle component of LC VCO used for frequency fine tuning. Accumulation mode MOS varactors were used to tune the oscillation frequency. MOS-based varactor is used due to a wide tuning range and higher Q factor, pMOS varactor has gate connected to the control voltage and drain, source, and bulk connected together to form the other terminal of the capacitor. The connection is reversed in nMOS as shown in Figure. 3. In accumulation mode majority carriers (holes) form a bottom plate of a parallel plate capacitance. In depletion, the presence of a depletion region with dopants atoms creates a non-linear capacitance that can be modeled as two series capacitances Cdepletion and Cox , which effectively increasing the plate thickness to tox + tdep. capacitor value of pmos varactor is ranges form
Cvar,min = 0.46 pF and *Cvar,max* = 0.86 pF.

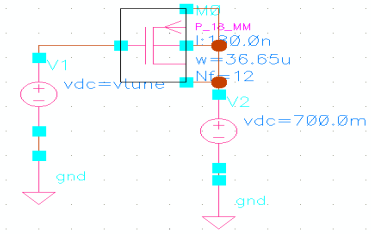


Figure: 4 PMOS Varactor

2. 3. A Proposed Schematic for LC-VCO

An LC-VCO is a combination of a resonator and an energy restoration device. The latter compensates for the tank loss to enable to a constant amplitude oscillation. Figure 4. shows the block diagram of the proposed LC VCO circuit, where a Low and stable phase noise fully integrated VCO were realized. This VCO was consisted by VCO core, constant current source, and variable current source. The variable current source was controlled by control voltage which was provided by a voltage to current converter circuit.

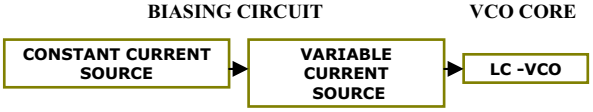


Figure: 5

The VCO physical parameters to be found in the design flow are: the inductance value and its parasitic, the varactor's value and its characteristics, the size of the pMOS and nMOS transistors and the size of the bias current pMOS transistors. A pMOS transistor has less 1/f noise, so a pMOS current source will mix a less power to the fundamentals. Using both pMOS and nMOS differential pairs can lower the current consumption of the oscillator. By connecting the outputs to the inputs the amplifier starts to amplify the noise at its inputs around the resonance frequency of the tank provided that its open loop gain G(ù) is greater than unity . Noise at other frequencies gets filtered out by the LC tank. This filtering characteristic has made the LC VCO the best in terms of phase noise performance. Figure5 shows the schematic of proposed LC VCO.
A cross coupled differential transistor pair provides a negative transconductance which is connected to LC-tank to cancel the loss. The capacitance in the feedback loop is composed of a pMOS transistors. During oscillation the capacitance changes abruptly, since capacitance switches between inversion and accumulation. The switching cycle frequency is determined by the control voltage.

2.4 Biasing circuit

This Biasing circuit was consisted by constant current source, and variable current source. The variable current source was controlled by control voltage which was provided by a voltage to current converter circuit. The bias current, Ibias, is steered between I1 and I3 by the differential pair consisting of identical transistors M3 and M4 with the steering controlled input voltages.

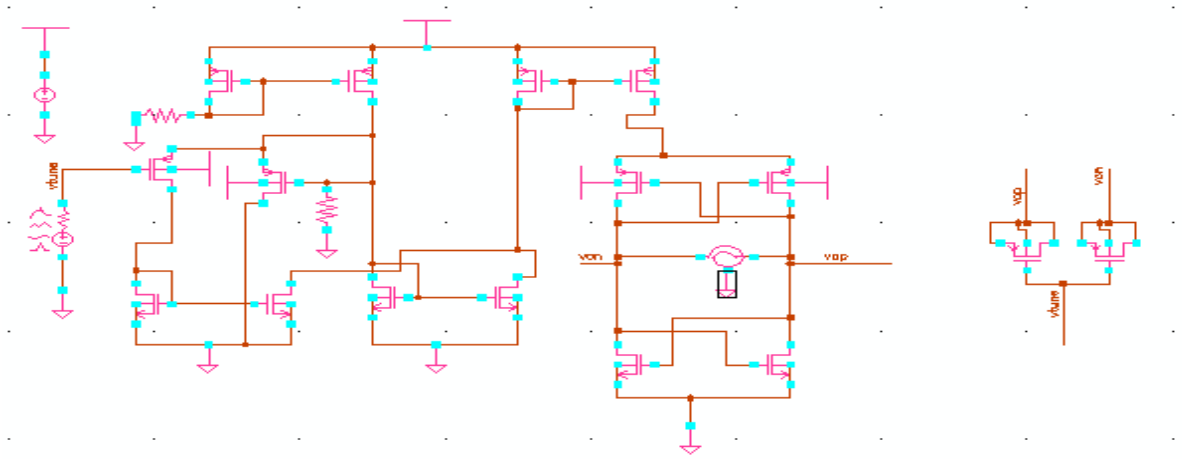


Figure: 6 UWB LC-VCO

The current from M3 is reflect in to the M9 drain of M4 is connected to the ground and one part of the Ibias i.e. I2 is go into the M7 and reflect into theM8 . gate of transistor M4 is connected to the high resistance The three current mirrors M5, M6 and M7, M8 beside M9 and M10 are used to generate output current that is proportional to the difference between the two differential drain currents I1 and I2 To implement this function we design the circuit in CMOS 0.18 µm technology. All transistors work in saturation mode for the specified output current level. The design procedure starts by adjusting the DC potential level at the gate of the bias current source M2 and at the output at half the supply voltage with both inputs shorted to ground.
The current mirrors allow current to flow only in one direction. However, by placing a P-mirror on top of an Nmirror we can get a bi-directional current mirror which is convenient for realizing weights. With the steering controlled by the voltage difference of the input voltages, and the current mirrors. We know that the saturation current is:

$$I = K_p/2(Vgs - Vt)^2$$

Where *Kp* is a material constant.
Applying this expression to the proposed circuit diagram M6 &M8 transistors using the current mirror ratio 1:1 we find

$$I1 = 0.5\, I_{bias}(1 + I_{out}/I_{bias}) \qquad I2 = 0.5\, I_{bias}(1 - I_{out}/I_{bias})$$

The sum of the two drain currents must be equal to the bias current

I_{bias} = I1 + I2

Then

$V_{tune} = I_{out}/\sqrt{K_p} \times I_{bias}$

The trance conductance G of the is just the slope of the output current versus the input voltage curve.

G = Iout/Vtune = $\sqrt{K_p} \times I_{bias}$

Notice that the transconductace is proportional to the bias I bias, a fact that will become important when the amplifier is used to produce a voltage type output is designed to be a function of the voltage difference and I bias, independent of any devices connected, such as loads or the current mirror. To obtain the current output as this difference, the current mirror is used along at the output node so that I out to the difference of the transistor currents. The function of I out versus the voltage difference realized depends upon the MOS transistors and their modes of operation used to form the current difference.

1. **Phase noise :** The importance of phase noise in wireless communications comes from the fact that if the local oscillator output contains phase noise, both up/down converted signals in the transceiver will be corrupted.

It is essentially a random deviation in frequency which can also be viewed as a random variation in the zero crossing points of the time-dependent oscillator waveform. Phase noise and jitter are two related quantities associated with a noisy oscillator, where phase noise is a frequency-domain view of the noise spectrum around the oscillator signal, while jitter is a time domain measure of the timing accuracy of the oscillator period.

$V_n^2 = KT\gamma g_m Q_L R_L(\omega 0/\Delta\omega)$

Phase noise is

$N_{phase} = 8 \times V_n^2/V_{signal}$

Where I is the bias current, γ is a factor equals from 2 to 3, K is Boltzmann constant and T is the absolute temperature, which means that signal power can be increased either by higher Q or by higher L. Phase noise also, can be improved by high Q. The VCO performance can be compared by means of a figure of merit (FOM) , which may be given by:

$$VCO\ (FOM) = \emptyset(t)\frac{dBc}{Hz} - \frac{20logf_{osc}}{f_{offset}} + 10logP_{diss}/1mW$$

Where f_{osc} is the carrier frequency, f_{offset} is the frequency offset, Pdiss is the power consumed by the VCO core, and Φ (t) is the phase noise simulated at an offset from the carrier.

III. Design Parameters

Design Parameters	
Inductor (L)	1.5nH
Varactor	
Cvar,min	0.46 pF
Cvar,max	0.86 pF
W/L	36.65/0.18 u, N.F.=12
VCO -Transistor	
W/L(PMOS)	52/0.18u
W/L(NMOS)	17/0.18u
gm	1.2mS
V(supply)	1.2
Oscillation frequency	5.7GHz

Table:1

IV.. Simulation Results

1. C-V curve of A-MOS varactor

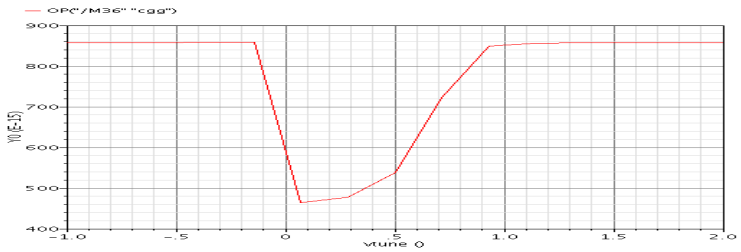


Figure: 7

2. DC Response of Biasing Circuit shows the graph between output current and input voltage and the slope of 148uS is found.

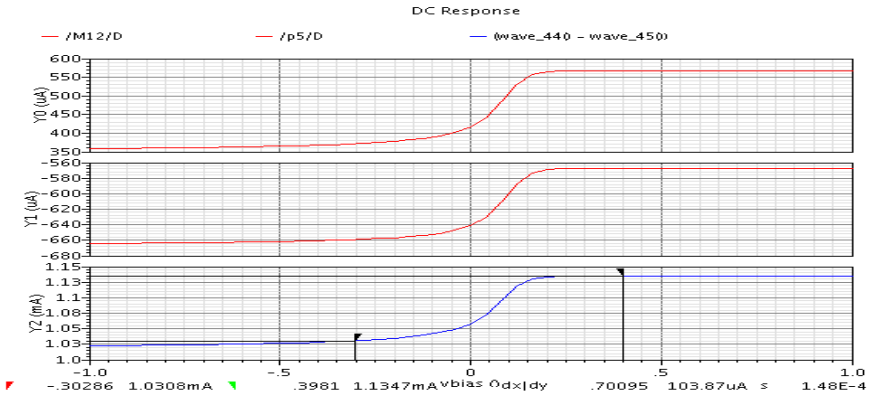


Figure: 8

4.1 VCO Output responses:

VCO steady-state and extracting its characteristics (oscillation frequency, power spectra, phase noise,etc.) has become one of the most critical challenges in the design flow. Simulation has been performed with 1.2 V power supply voltage. The simulator used was Cadence UMC 0.18u technology

Parameter	Simulation results	[30]
Supply Voltage	1.2V	1.2V
Current Consumption	2.557mA	2.7mA
Operating Frequency	5.7GHz	5.7GHz
Power Consumption	3.068mW	3.24mW
Tuning Range	5.47-6.6GHz ,18.7%	5.07-5.77GHz ,20%
O/P POWER	7.02dBm	Not given
Phase Noise @1MHz offset frequency with 5.7GHz carrier	-113.7 dBc/Hz	-92 dBc/Hz

Table: 2

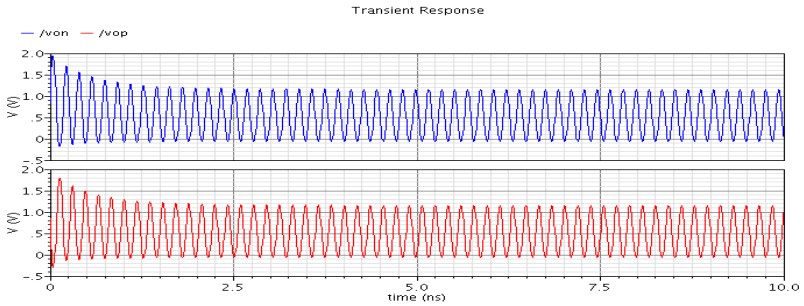
From the designed UWB VCO current consumption in the whole circuit is 2.557mA is found with the supply voltage of 1.2V.

DFT of the response shows the value of output voltage is0.56 at frequency =0Hz and the harmonic frequency at various value of control voltage are as follows:

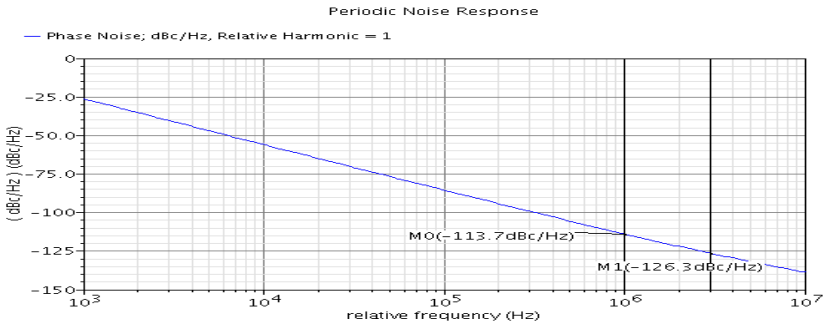
at vtune=0 V, harmonic frequency =5.47GHz, vtune=0.822 V, harmonic frequency =5.7GHz, vtune=1.2V, harmonic frequency =6.06GHz

Simulated phase noise displayed by the VCO at the maximum and minimum oscillation frequencies, where the flicker (1/f) noise of the current source is the main source of the phase noise. Inductance L is 1.5nH, and the total capacitance is in the range of 0.46pF to 0.86 pF. most commonly used unit for phase noise is power below the

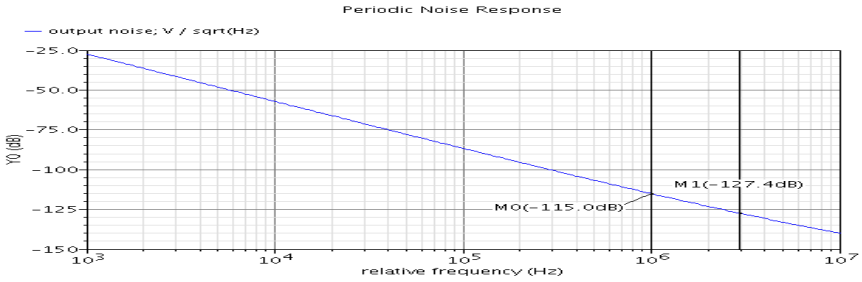
carrier per Hertz, expressed in dB, or dBc/Hz, at some offset frequency Äù from the carrier frequency ù0. The phase noise at 1MHz offset from the carrier is - 113.7dBc/Hz. Figure shows the simulated oscillation frequency against control voltage.



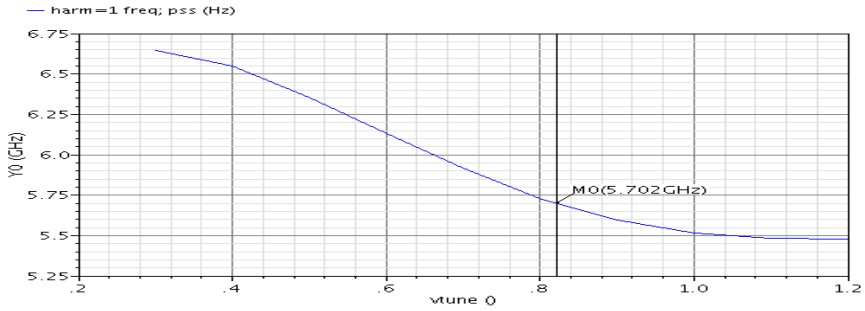
3.Transient response



4.Phase noise response of the circuit.



5.Output noise of the circuit:



6. Control voltage v/s frequency curve.

Figure: 9

V. CONCLUSION

A 5.7-GHz fully integrated, LC voltage-controlled oscillator (VCO) using Cadence UMC 1800nm MOS transistors is successfully synthesized. The simulated phase-noise values are found to be -113.7 dBc/Hz at 1MHz offset from 5.7 GH carriers. The VCO consumes 2.557mA from a 1.2V supply. The accumulation-mode MOS varactor tuning is used to achieve 18.7% tuning range. Those result shows that a good trade-off between phase noise & power consumption is reached.

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