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A NOVEL REVERSE CONVERTER FOR A NEW LENGTH-3 MODULI SET $\{2^{2n+2}-1,2^{2n+1}-1,2^{2n+1}\}$

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Abstract-In this paper, a novel length-3 moduli set $\{2^{2n+2}-1,2^{2n+1}-1,2^{2n+1}\}$ with its associated adder based reverse converter is presented. The proposed moduli set provides 75% larger Dynamic Range, for the same n value when compared with state of the art counterparts. Additionally, it possesses some interesting number theoretic properties which makes it suitable for the realization of an efficient reverse converter based on the New Chinese Remainder Theorem. Theoretically speaking, the resulting residue to binary converter has a delay of $(6n+7)t_{FA}+2t_{MUX}$ with an area cost of $(12n+10)$ FA, which substantially outperforms state of the art equivalent reverse converters. To assess the practical implications of our proposal we implemented it and equivalent state of the art counterparts in FPGA. The experimental results indicate that on average, our proposal reduces the hardware resource requirements by 34%, while being 19% faster.

Keywords- Residue Number System (RNS), Computer Architecture, Moduli Set, Dynamic Range, Reverse Converter,

I. INTRODUCTION

Residue Number System (RNS) is a non-weighted integer number system that supports carry free addition, borrow free subtraction, and digit by digit multiplication without the generation of partial products. This makes it a good candidate for high performance, low power consumption, fault-tolerant computing, and secure Digital Signal Processing (DSP) applications [1]. For this reason, RNS has received considerable attention in DSP applications requiring intensive computations e.g., digital filtering, Fast Fourier Transform, Discrete Cosine Transform and so on [2]. DSP hardware based on RNS is becoming an important factor in obtaining high speed and high precision at low cost [3].

The major issues in the efficient design of RNS based processors are: moduli set selection, residue arithmetic unit, and Data conversion [4]. The main obstacle to the widely utilization of RNS has to do with the following difficult RNS arithmetic operations: magnitude comparison, overflow detection, division, sign detection, moduli set selection, forward conversion, and reverse conversion. It is worth noting that, for a successful RNS implementation, moduli set selection and reverse conversion are the most critical issues [3], [5]. Thus, a carefully selected moduli set with its efficient associated reverse converter could improve the overall performance of the RNS architecture and therefore increase its applicability [4]. Each RNS architecture is based on a moduli set, which involves a set of pair-wise relatively prime integers and, the RNS architecture complexity and speed heavily depends on the selected moduli set [5].

As mentioned earlier, the key to any successful RNS based processor design, is how efficiently RNS to binary conversions can be performed. Up to date, many reverse conversion algorithms have been proposed for different classes of moduli sets, and each one of them has been claimed to be advantageous in certain cases.For e.g., $\{2^n,2^n-1,2^n+1\}$ [6], [7], $\{2^n,2^n-1,2^{n-1}-1\}$ [8], $\{2^{n+1}+1,2^{n+1}-1,2^n\}$ [9], $\{2^n,2^{2n}-1,2^{2n}+1\}$ [10] with their associated residue to binary converters have been proposed. Recently, $\{2^{2n+2}-1,2^{2n+1}-1,2^n\}$ moduli set with $5n$ bit Dynamic Range (DR) and its associated residue to binary converter has been proposed in [11], while an improved converter was introduced in [12].

Given that applications requiring larger DR than the moduli set $\{2^{2n+2}-1,2^{2n+1}-1,2^n\}$ are of practical interest, we present in this paper a novel moduli set $\{2^{2n+2}-1,2^{2n+1}-1,2^{2n+1}\}$ and its associated reverse conversion algorithm. The proposed moduli set has a larger DR and it is more balanced when compared with $\{2^{2n+2}-1,2^{2n+1}-1,2^n\}$, and exhibits some interesting number theoretic properties that enable effective reverse converter architectural design. The choice of this moduli set is for overcoming the intensive modulo operations involved in the implementation of most state of the art reverse converter algorithms and in the same time to provide a larger DR for length 3 moduli sets. The proposed reverse converter is

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based on the New Chinese Remainder Theorem (New CRT I) and has a delay of $(6n+7)t_{FA}+2t_{MUX}$ with an area cost of $(12n+10)$ FA, where t_{FA}, t_{MUX}, and FA area Full Adder delay, $2:1$ Multiplexer delay, and Full adder are, respectively. Theoretically speaking, our proposed reverse converter substantially outperforms existing equivalent state of the art in terms of area and delay for a substantially larger DR. To assess the practical implications of our proposal we implemented it and equivalent state of the art counterparts in FPGA. The experimental results suggest that, on average our scheme reduces the area requirements by 34% and is about 19% faster.

The remaining of this paper is structured as follows. In Section II, a brief background on reverse conversion methods is presented. The novel moduli set is introduced in Section III and the associated reverse conversion technique is presented in Section IV. Section V describes the hardware implementation of the proposed scheme and theoretically evaluates and compares its performance against existing state of the arts. In Section VI, we present an experimental assessment of the efficiency of the proposed and related state of the art converter. This paper is concluded with some final remarks in Section VII.

II. BACKGROUND

RNS is defined in terms of a set of relatively prime moduli set $\{m_i\}_{i=1,k}$, such that $gcd(m_i,m_j)=1$ for $i\neq j$, where $gcd(m_i,m_j)$ means the greatest common divisor of m_i and m_j, while $M=\prod_{i=1}^{k}m_i$, is the DR. The residues of a decimal number X can be derived as $x_i=|X|_{m_i}$, this implies that X can be represented in RNS as $X=(x_1,x_2,x_3,...,x_k),0\le x_i<m_i$. It is important to note that this representation is unique for any integer $X\in[0,M-1]$ and that $|X|_{m_i}$ denotes X mod m_i operation and is defined as $X=x_i+bm_i$ for some integer $b \ni 0\le x_i<m_i$. Given a moduli set $\{m_i\}_{i=1,k}$, to convert residues $(x_1,x_2,...,x_k)$ into its corresponding decimal number X, the traditional CRT, New CRTs, and Mixed Radix Conversion (MRC) are generally used [3]. For the CRT, the decimal number X is computed as:

$$X=\left|\sum_{i=1}^{k}m_i\left|M_i^{-1}\right|_{m_i}x_i\right|_M \tag{1}$$

where $M=\prod_{i=1}^{k}m_i$, $M_i=\dfrac{M}{m_i}$ and M_i^{-1} is the multiplicative inverse of M_i with respect to m_i.

Alternatively, given a moduli set $\{m_i\}_{i=1,3}$, the residues (x_1,x_2,x_3) can be converted into the corresponding decimal number X using the New CRT I as follows [14]:

$$X=x_1+m_1\left|k_1(x_2-x_1)+k_2m_2(x_3-x_2)\right|_{m_2m_3}, \tag{2}$$

where,

$$\left|k_1m_1\right|_{m_2m_3}=1, \tag{3}$$

$$\left|k_2m_1m_2\right|_{m_3}=1. \tag{4}$$

III. $\{2^{2n+2}-1,2^{2n+1}-1,2^{2n+1}\}$ MODULI SET

For a given RNS moduli set to be valid, it is required that all the elements in the moduli set are co-prime. Thus, in order to prove that the proposed set can be utilized for the construction of a valid RNS architecture, we have to demonstrate that the moduli $2^{2n+2}-1,2^{2n+1}-1$, and 2^{2n+1} are pair-wise relatively prime.

Theorem 1 *The moduli* $2^{2n+2}-1,2^{2n+1}-1$, *and* 2^{2n+1} *are pair-wise relatively prime numbers.*

Proof. It has already been demonstrated that $gcd(2^{2n+2}-1,2^{2n+1}-1)=1$, and $gcd(2^{2n+1}-1,2^{2n+1})=1$ in [11] and

[13], respectively. We therefore need to only show that $2^{2n+2}-1$ and 2^{2n+1} are coprime. From the Euclidean theorem, $gcd(a,b)=gcd(b,|a|_b)$, therefore, $gcd(2^{2n+2}-1,2^{2n+1})=gcd(2^{2n+1},|(2^{2n+2}-1|_{2^{2n+1}})=gcd(2^{2n+1},-1)=1$. Thus, from these results, it can be concluded that, $\{2^{2n+2}-1,2^{2n+1}-1,2^{2n+1}\}$ moduli set contains relatively prime numbers and it is a valid RNS moduli set. □

IV. REVERSE CONVERSION TECHNIQUE

Given the residues (x_1,x_2,x_3) with respect to the moduli set $\{2^{2n+2}-1,2^{2n+1}-1,2^{2n+1}\}$, we present a NEW CRT 1 based residue to binary converter as follows:

Theorem 2 *Considering the proposed moduli set* $\{2^{2n+1},2^{2n+1}-1,2^{2n+2}-1\}$*, the following holds true:*

$$k_1=\left|(2^{2n+1})^{-1}\right|_{(2^{2n+1}-1)(2^{2n+2}-1)}=-(2^{2n+2}-3) \tag{5}$$

$$k_2=\left|((2^{2n+1})(2^{2n+1}-1))^{-1}\right|_{2^{2n+2}-1}=-4 \tag{6}$$

Proof. If it can be demonstrated that $\left|(2^{2n+1})(3-2^{2n+2})\right|_{2^{2n+1}-1}=1$, then $-(2^{2n+2}-3)$ is the multiplicative inverse of 2^{2n+1} with respect to $(2^{2n+1}-1)(2^{2n+2}-1)$. $\left|(2^{2n+1})(3-2^{2n+2})\right|_{(2^{2n+1}-1)(2^{2n+2}-1)}=1$, thus, Equation (5) holds true. Similarly, if $\left|(2^{2n+1})(2^{2n+1}-1)\times-4\right|_{2^{2n+2}-1}=1$, then -4 is the multiplicative inverse of $(2^{2n+1})(2^{2n+1}-1)$ with respect to $2^{2n+2}-1$. $\left|(2^{2n+1})(2^{2n+1}-1)\times-4\right|_{2^{2n+2}-1}=\left|2^{2n+3}-2^{4n+4}\right|_{2^{2n+2}-1}=\left|2-1\right|_{2^{2n+2}-1}=1$, Thus, Equation (6) also holds true. □

Theorem 3 *For the moduli set* $\{2^{2n+1},2^{2n+1}-1,2^{2n+2}-1\}$*, the decimal equivalent of the RNS number* (x_1,x_2,x_3) *can be computed as follows:*

$$X=x_1+2^{2n+1}\gamma \tag{7}$$

where,

$$\gamma=2^{2n+1}T-T+\omega \tag{8}$$

$$T=\left|(2^2x_1-2^2x_3+2\omega)\right|_{2^{2n+2}-1} \tag{9}$$

$$\omega=\left|(x_2-x_1)\right|_{2^{2n+1}-1} \tag{10}$$

Proof. Let $m_1=2^{2n+1},m_2=2^{2n+1}-1,$ and $m_3=2^{2n+2}-1$. Substituting these values of m_1,m_2,m_3 and that of k_1 and k_2 from (5) and (6), respectively, into (2), we obtain:

$$X=x_1+2^{2n+1}\Big|-(2^{2n+2}-3)(x_2-x_1)$$
$$-2^2(2^{2n+1}-1)(x_3-x_2)\Big|_{(2^{2n+1}-1)(2^{2n+2}-1)}, \tag{11}$$

Rewriting (11), we have:

$$X=x_1+2^{2n+1}|T|_{(2^{2n+1}-1)(2^{2n+2}-1)}, \tag{12}$$

where,

$$T=-(2^{2n+2}-3)(x_2-x_1)-2^2(2^{2n+1}-1)(x_3-x_2),$$

Applying the property: $|T|_{m_1 m_2} = m_1 \left\| \left\lfloor \frac{T}{m_1} \right\rfloor \right\|_{m_2} + |T|_{m_1}$ [15] to (12), and simplifying further, we obtain:

$$X = x_1 + (2^{2n+1})\gamma \tag{13}$$

where,

$$\gamma = (2^{2n+1}-1)\Big|-2^2(x_2 - x_1) + 2|x_2 - x_1|_{2^{2n+1}-1} - 2^2(x_3 - x_2)\Big|_{(2^{2n+2}-1)} + |x_2 - x_1|_{2^{2n+1}-1} \tag{14}$$

For the sake of completeness, we have:

$$\gamma = (2^{2n+1}-1)T + \omega \tag{15}$$

$$T = \Big|-2^2(x_2 - x_1) + 2|x_2 - x_1|_{2^{2n+1}-1} - 2^2(x_3 - x_2)\Big|_{(2^{2n+2}-1)} \tag{16}$$

$$\omega = |x_2 - x_1|_{2^{2n+1}-1} \tag{17}$$

It can be observed that (16) can be further simplified to obtain:

$$T = \left|2^2 x_1 - 2^2 x_3 + 2\omega\right|_{2^{2n+2}-1} \quad \square \tag{18}$$

We proceed to further reduce the hardware complexity of (13) by utilizing the following properties [6]:

Property 1: The multiplication of a residue number by 2^k in modulo $(2^p - 1)$ is computed by k bit circular left shifting

Property 2: A negative number in modulo $(2^p - 1)$ is calculated by subtracting the number in question from $(2^p - 1)$. In binary representation, the ones complement of the number gives the result.

Let the residues (x_1, x_2, x_3) have binary representation as follows:

$$x_1 = (\underbrace{x_{1,2n} x_{1,2n-1} \ldots x_{1,1} x_{1,0}}_{2n+1}) \tag{19}$$

$$x_2 = (\underbrace{x_{2,2n} x_{2,n-1} \ldots x_{2,1} x_{2,0}}_{2n+1}) \tag{20}$$

$$x_3 = (\underbrace{x_{3,2n+1} x_{3,2n} \ldots x_{3,1} x_{3,0}}_{2n+2}) \tag{21}$$

Rewriting (18) and simplifying the various parameters using properties 1 and 2, we obtain: $T = |r_1 + r_2 + 2\omega|_{2^{2n+2}-1}$, $2\omega = r_3^{'} + r_3^{''}$ therefore $T = |r_1 + r_2 + r_3^{'} + r_3^{''}|_{2^{2n+2}-1}$.

$$r_1 = |2^2 x_1|_{2^{2n+2}-1} = \underbrace{x_{1,2n-1} x_{1,2n-2} \ldots x_{1,0}\, 0\, x_{1,2n}}_{2n+2} \tag{22}$$

$$r_2 = |-2^2 x_3|_{2^{2n+2}-1} = \underbrace{\bar{x}_{3,2n-1} \bar{x}_{3,2n-2} \ldots \bar{x}_{3,0}\, \bar{x}_{3,2n+1}\, \bar{x}_{3,2n}}_{2n+2} \tag{23}$$

$$r_3^{'} = \Big||x_2|_{2^{2n+1}-1}\Big|_{2^{2n+2}-1}$$

$$= \underbrace{x_{2,2n}x_{2,2n-1}...x_{2,0}0}_{2n+2} \quad (24)$$

$$r_3'' = \left\| -x_1 \right|_{2^{2n+1}-1} \Big|_{2^{2n+2}-1}$$
$$= \underbrace{\bar{x}_{1,2n}\bar{x}_{1,2n-1}...\bar{x}_{1,0}1}_{2n+2} \quad (25)$$

Similarly, from (17):

$$\omega = \left| x_2 - x_1 \right|_{2^{2n+1}-1}$$
$$= \omega' + \omega'' \quad (26)$$

$$\omega' = \underbrace{x_{2,2n}x_{2,2n-1}...x_{2,0}}_{2n+1} \quad (27)$$

$$\omega'' = \underbrace{\bar{x}_{1,2n}\bar{x}_{1,2n-1}...\bar{x}_{1,0}}_{2n+1} \quad (28)$$

V. HARDWARE REALIZATION AND PERFORMANCE ANALYSIS

The hardware structure of the proposed reverse converter for the novel moduli set $\{2^{2n+1}, 2^{2n+1}-1, 2^{2n+2}-1\}$ is based on (13). As it can be observed in Figure 1, the reverse converter architecture consists of a $(2n+1)$-bit and a $(2n+2)$-bit Carry Save Adder (CSA) with End Around Carry (EAC), a parallel $(2n+1)$-bit and $(2n+2)$-bit modulo $(2^{2n+1}-1)$ and $(2^{2n+2}-1)$ adder, respectively, and a $(4n+3)$-bit Carry Propagate Adder (CPA). First of all, the realization of (13) is the resultant of the reduction of modulo $(2^{2n+1}-1)(2^{2n+2}-1)$ operation in (12) into two parallel modulo operations $(2^{2n+1}-1)$ and $(2^{2n+2}-1)$. The reduction is without any hardware resource requirments. The parameters r_1, r_2, r_3' and r_3'' are added by two cascaded $(2n+2)$-bit CSAs with end around carry resulting in the values s_2 and c_2. These values are further reduced to one number T with CPA2. Similarly, in parallel ω' and ω'' are added with CPA1. To speed up these EAC parallel additions, we utilize anticipated computation, where $s_2 + c_2$ and $s_3 + c_3$ are computed for both $cin = 0$ and $cin = 1$, then we select the right result with a $2:1$ MUX. The implementation of (8) involves a $(4n+3)-$bit CPA. Finally, the computation of (7) is achieved simply by a concatenation operation, which does not require any additional hardware resources. From the above, it can be deduced that the proposed RNS to binary converter make use of $(12n+10)$ FA and has a delay of $(6n+7)t_{FA} + 2t_{MUX}$.

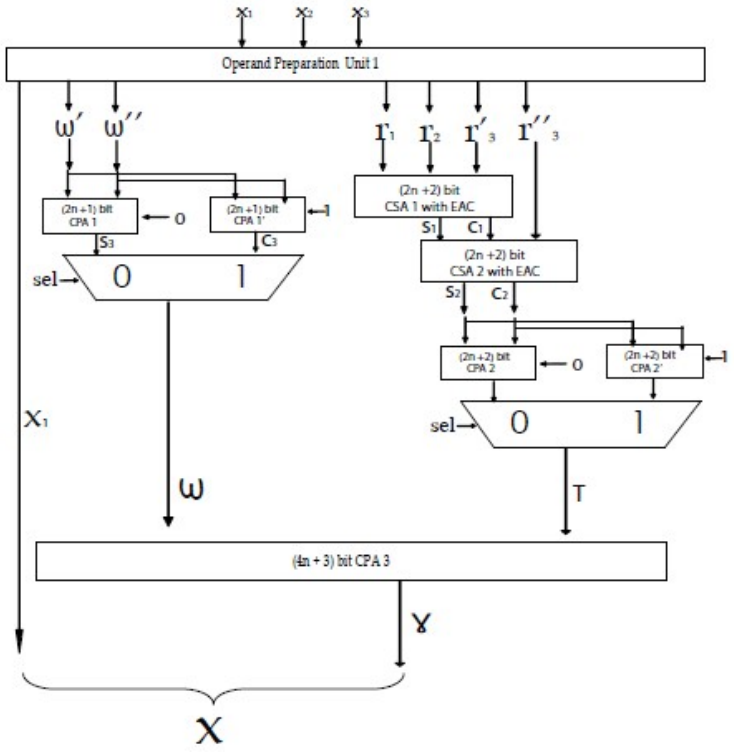
Next, we compare our reverse converter with equivalent best state of the art residue to binary converter presented in [13] in terms of both delay and hardware resources requirement. For the sake of completeness, we also include the reverse converters presented in [16] and [17] in the comparison to demonstrate that our scheme satisfactorily can compete with other state of the art reverse converters associated with length 4 moduli sets with $6n$ bit DR. We also note that the proposed moduli set provides a DR about 75% larger for the same n value when compared with state of the art counterparts. Theoretically speaking, the proposed scheme requires $(12n+10)$ FA hardware resources. Table I summarizes the area and delay of the considered converters and one can observe that our scheme outperforms the related state of the arts in terms of conversion time while requiring slightly larger area than [16] but substantially less area than those presented in [13] and [17].

Table 1: Theoretical Area and Delay Comparison

Converters	[13]	[16]	[17]	Proposed Converter
Moduli	$\{2^{2n+1}-1, 2^{2n+1}, 2^{2n}-1$	$\{2^n-1, 2^n+1, 2^{2n}, 2^{2n}+1$	$\{2^n+1, 2^n-1, 2^{2n}, 2^{2n+1}-1$	$\{2^{2n+1}, 2^{2n+1}-1, 2^{2n+2}-1$

Set				
Dynamic Range	$6n$ -bits	$6n$ -bits	$6n$ -bits	$6n$ -bits
FA	$(18n+3)$	$10n+6$	$16n+1$	$12n+10$
Delay	$(8n+6)t_{FA}+2t_{MUX}$	$(8n+3)t_{FA}$	$(8n+2)t_{FA}$	$(6n+7)t_{FA}+2t_{MUX}$

Figure 1: Block diagram for the Proposed Converter



VI. EXPERIMENTAL RESULTS

The circuits of the proposed and related best state of the art reverse converters were described in synthesizable VHDL and synthesized on Spartan 6 xc6slx45-3fgg484 FPGA with Xilinx ISE 14.3 for a wide range of n values. The performance of the converters were evaluated in terms of area expressed by the number of occupied slice LUTs and the delay in nano seconds (ns). The results are presented in Table 2 and indicate that on average, the proposed converter reduces the area by 34% and delay by 19% when compared with the one presented in [13]. In comparison with the reverse converter in [16], the proposed reverse converter reduces the area by 1.0%, while it is 4.15% faster. Similarly, with respect to the counterpart converter presented in [17], our scheme substantially reduces the area and the conversion delay by 34.17% and 33.29%, respectively.

Table 2: Experimental Delay and Area Comparison

	[16]		[17]		[13]		Proposed	
n	Delay	Area	Delay	Area	Delay	Area	Delay	Area
2	17.002	49	15.276	57	17.158	65	13.286	54
4	18.453	103	24.295	144	19.901	147	16.035	101
6	21.169	157	28.069	221	23.742	221	19.682	148
8	22.652	204	30.308	299	26.722	314	19.427	206
10	23.238	258	34.254	374	26.919	373	23.048	252
12	26.919	315	36.442	472	29.677	458	22.832	305
14	24.450	363	35.249	533	32.098	530	25.674	345
16	24.045	415	38.789	612	31.250	652	25.045	434
18	24.180	473	39.180	727	29.402	732	26.122	470
20	26.437	522	41.460	806	32.598	782	26.639	513

VII. CONCLUSIONS

In this paper, we proposed a novel moduli set with its associated reverse converter based on the New CRT. The proposed moduli set offers a DR about 75% larger for the same n values when compared with state of the art counterparts. Based on the interesting number theoretic properties inherent with the proposed moduli set, an efficient residue to binary converter is designed. From the theoretical point of view, our proposal outperforms the related state of the arts in terms of conversion time while requiring slightly larger area than [16] but substantially less area than [13] and [17]. Further, to also assess the practical implications, we implemented in FPGA the proposed scheme and state of the art counterparts.The digital circuits of the proposed and related best state of the art reverse converters were described in synthesizable VHDL and synthesized on Spartan 6 xc6slx45-3fgg484 FPGA with Xilinx ISE 14.3 for a wide range of n values. The experimental results presented in Table 2 suggests that, on average, the proposed converter reduces the hardware resource requirements by 34% and the conversion delay by 19% when compared with the one presented in [13]. Also, in terms of delay, our proposal is about 19% speed up of conversion time. Additionally, in comparison with the reverse converter presented in [16], our proposal reduces the area by 1.0%, while it is 4.15% faster. Similarly, with respect to the counterpart converter presented in [17], our scheme substantially reduces the area by 34.17% and the delay by 33.29%.

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