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MITIGATION OF HARMONICS IN MULTILEVEL INVERTER USING MSPWM & SVM TECHNIQUES

Dr.S.Sivakumar[1], S.Sowmiya[2] and S.Shangeetha[3]

Abstract- Cascaded Multilevel inverters are getting to be noticeably well known in the field of high power applications. These inverters delivers high power at the output side are favoured for industrial applications. This paper is chiefly focused on Modified Cascaded Multilevel inverter with decreased switches and harmonics. The control signals to the gate are engendered using MSPWM and SVM techniques. The objective of this paper is to diminish switches with increase in multilevel outputs which inherently reduces the cost and harmonics. The inverter is designed and developed in MATLAB® Simulink platform and results are obtained. The examination has been made on Total Harmonic Distortion (THD). The frame work prototype is developed using Power MOSFET Switches and THD is examined using Power Quality Analyser. The results are validated in both Simulation and Hardware.

Keywords **– Cascaded Multilevel Inverter, Multiple Sinusoidal Pulse Width Modulation (MSPWM) and Space Vector Modulation (SVM), Total Harmonic Distortion (THD)**

I. INTRODUCTION

Multilevel inverter is utilized ordinarily in the field of Power electronic industries because of its high reliability. Multilevel inverters are exceptionally dependable, exceedingly adaptable, high conversion efficiency, flexible adaptable to improve, low output switching frequency, low cost and the Switching losses is very less in semiconductor switches because of this favourable circumstances the multilevel inverters are well emerged trends in the area of high power applications. When the output level of MLI increases, the switching devices are increased. So the electromagnetic interference conduction noise levels are increased, although the output waveform is similar to sinusoidal and it has less THD.[8]

The different topologies of Multilevel inverter includes Capacitor clamped MLI, Diode clamped MLI, Cascaded MLI [3][4] type. All these topologies are used in different applications. In diode clamped MLI the cost is low but more than three levels the output gets limited. In Capacitor clamped MLI the capacitors have to be pre charged before using it. But Cascaded MLI produce different voltage level and it is easier to analyze. Cascaded multilevel inverters are used in motor drives and in electric vehicle drives. Hence for industrial applications cascaded MLI plays a major role. The seven level output is obtained by the conventional cascaded MLI shown in fig 1 which consists of 12 semiconductor switches. In this proposed cascaded MLI shown in fig 2, 7 switches and 3 diodes are used for seven level output. The multiple sinusoidal and space vector modulation strategies are used in this paper.

[1] *Department of Electrical and Electronics Engineering Kings College of Engineering, Thanjavur*
[2] *Department of Electrical and Electronics Engineering Kings College of Engineering, Thanjavur*
[3] *Department of Computer Science and Engineering, Kings College of Engineering, Thanjavur*

II. CONVENTIONAL CASCADED MULTILEVEL INVERTER

The conventional cascaded multilevel inverter consists of 2 or more full converter. The full converter has 4 semiconductor switches which are triggered in order to get multilevel output. There are 3 separate DC sources, 12 semiconductor switches in a general 7 level MLI shown in fig 1.

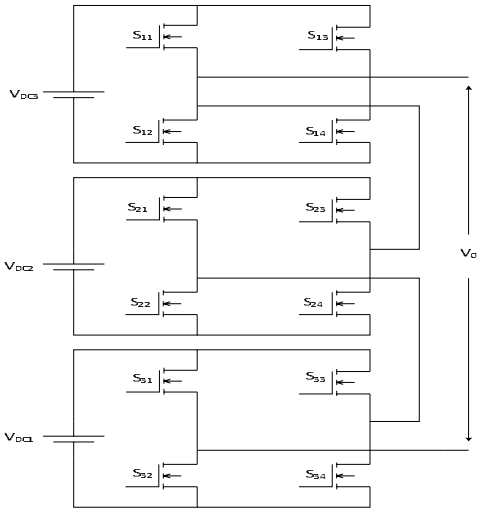


Fig:1 General Cascaded MLI Circuit

The circuit has 3 dc sources $V_{DC1,}$ $V_{DC2,}$ $V_{DC3,}$ and 4 switches for each bridge. The first bridge has power semiconductor switches namely S_{11}, S_{12}, S_{13}, S_{14} and for second bridge S_{21}, S_{22}, S_{23}, S_{24} are the power semiconductor switches and for third bridge S_{31}, S_{32}, S_{33}, S_{34} are the power semiconductor switches. The output voltage V_0 can be obtained across the first and third bridge. As the switches used in the conventional cascaded multilevel inverter is high, the cost and the switching losses tend to become higher.

III. MODIFIED CASCADED MULTILEVEL INVERTER

In a modified cascaded multilevel inverter shown in fig 2, the switching losses becomes less because it has only 7 Power MOSFET switches and 3 power diodes. The intricacy of the circuit is reduced because of less usage of switches. Moreover the modified cascaded MLI was more economical when compared to general cascaded MLI.

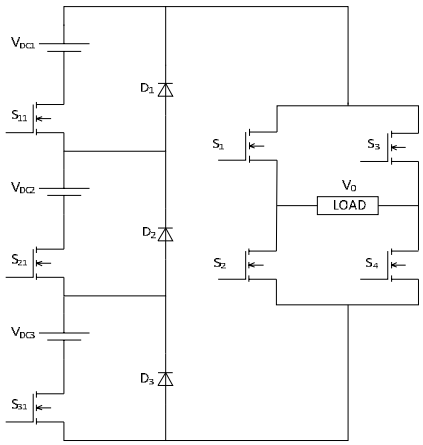


Fig: 2 Modified Cascaded MLI with Reduced Switches

The circuit has 3 separate DC sources namely V_{DC1}, V_{DC2} and V_{DC3} and the main power switches are S_{11}, S_{21}, S_{31} and for H-bridge S_1, S_2, S_3 and S_4 are used which is for inverter operation.

Duration	ON Switches	ON Diodes	Voltage Levels
Positive Half Cycle	-	D_1, D_2, D_3	0
	S_{11}	D_2, D_3	$+V_{DC}$
	S_{11}, S_{21}	D_3	$+2V_{DC}$
	S_{11}, S_{21}, S_{31}	-	$+3V_{DC}$
Negative Half Cycle	-	D_1, D_2, D_3	0
	S_{11}	D_2, D_3	$-V_{DC}$
	S_{11}, S_{21}	D_3	$-2V_{DC}$
	S_{11}, S_{21}, S_{31}	-	$-3V_{DC}$

Table.1: Switching Table for Modified Cascaded Multilevel inverter

IV. OPERATION OF MODIFIED CASCADED MLI

The conversion unit of the proposed inverter has a power switching device in series with the voltage source and a diode. The number of output levels depends on the number of conversion unit. The output V_{DC} is obtained when triggering S_{11}. Similarly $+2V_{DC}$ is obtained as output voltage as a addition of V_{DC1} and V_{DC2} when triggering S_{11} and $S_{21.}$ The output $+3V_{DC}$ is obtained when all the switches are triggered together.

The unidirectional output levels are converted into bidirectional with the use of H-bridge. In the H-bridge, S_1 and S_4 are ON during positive half cycle and S_2 and S_3 are ON during negative half cycle. Table 1 shows the operation of switches during positive and negative half cycle. The output waveform of modified cascaded multilevel inverter is shown in fig 6.

The number of output levels = 1 + (2* Number of DC sources)

V. MODULATION STRATEGIES

I) MSPWM Strategy

The multiple sinusoidal signals are compared with the carrier signal in order to get the desired pulse width [2][5]. The gate pulses are obtained by comparing three sinusoidal waveforms with a single carrier. The output frequency is same as that of the reference waveform.

The frequency modulation and the amplitude modulation are given by

$M_f = f_c / f_m$

$M_a = 2A_m / (N-1)\,Ac$

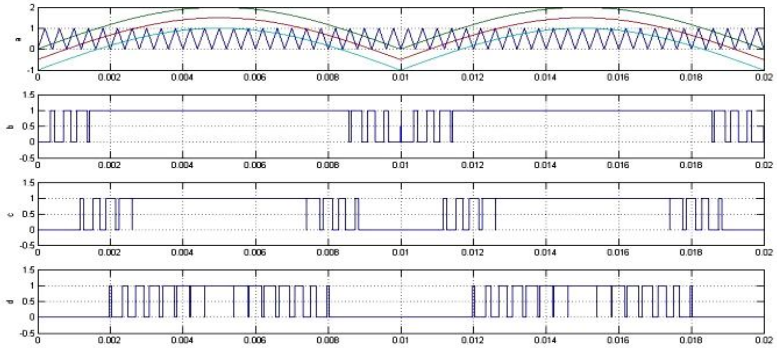
Where f_c = frequency of the carrier signal.

f_m = frequency of the modulating signal.

A_c = amplitude of the carrier signal.

A_m = amplitude of the modulating signal.

N = number of levels.



III) SVPWM Strategy

The reference signal is sampled regularly for multiphase ac generation in space vector PWM technique [1][7]. Switching control signals are produced by the SVPWM technique. SVPWM provides low current ripple, low output harmonic distortions when compared with sinusoidal PWM. Also hardware implementation of SVPWM is quite easier.

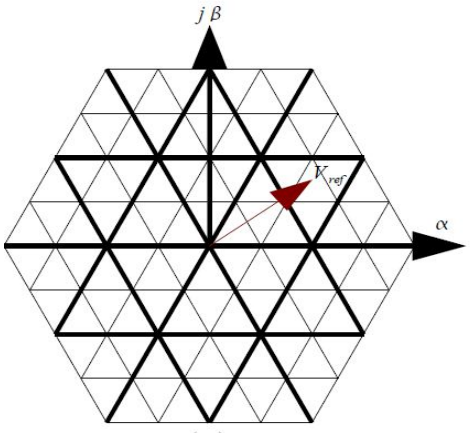


Fig: 3 Space Vector diagram of a multilevel inverter

The αβ-plane represents the reference vector. The three- dimensional plane is transformed into two dimensional plane which consist the vectors of the three phases. The switches being ON or OFF are determined by the location of the reference vector on this αβ-plane [7].

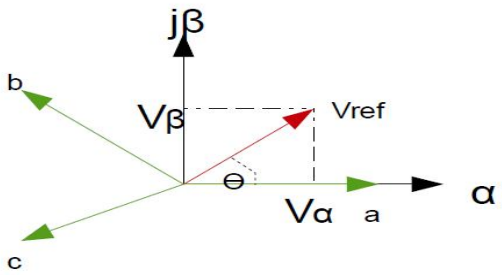


Fig: 4 Reference vector in the two and three dimensional plane

VI. SIMULATION RESULTS

Before hardware implementation the circuit is implemented through MATLAB/SIMULINK. . The seven level inverter circuit is simulated in fig.5 and results of output voltage and THD is shown in fig.6

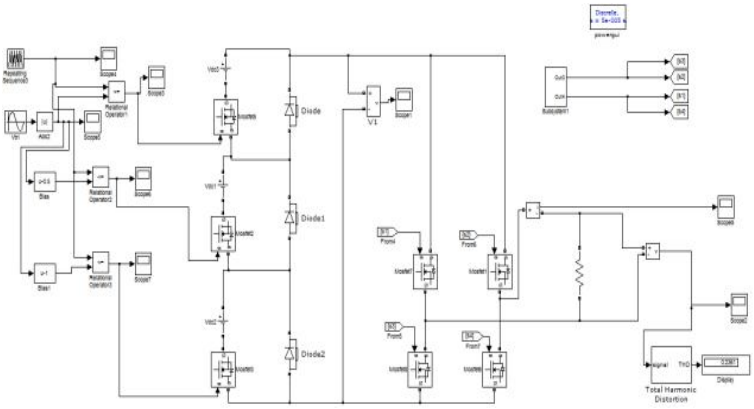


Fig: 7 MATLAB/Simulink Model of Modified Cascaded 7-Level Inverter (MSPWM)

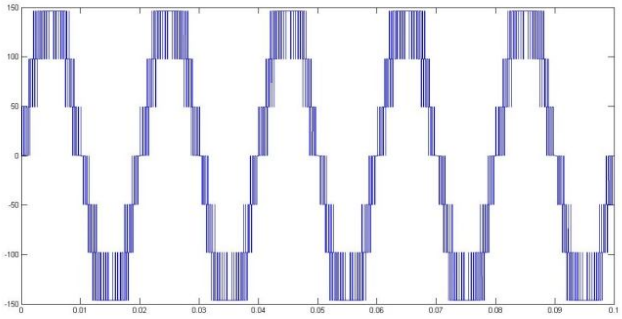


Fig: 8 Seven level output for MSPWM

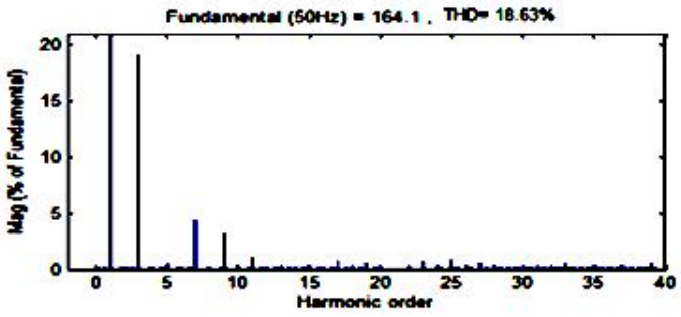


Fig: 9 FFT Analysis for MSPWM

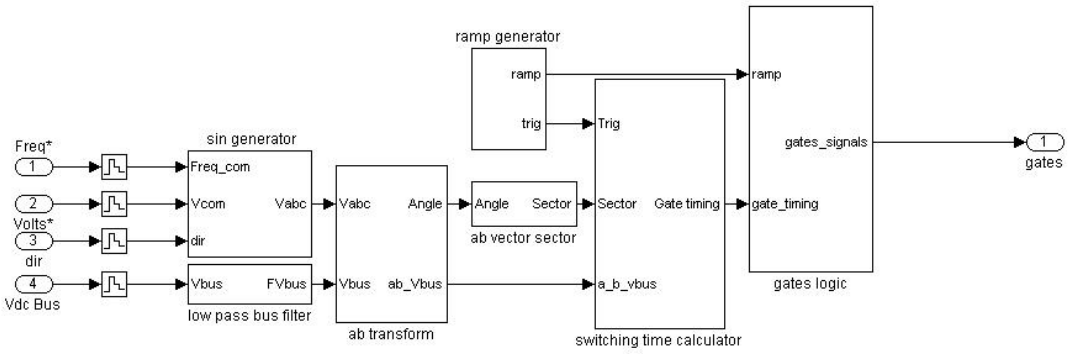


Fig: 10 Gate pulse generation of SVPWM

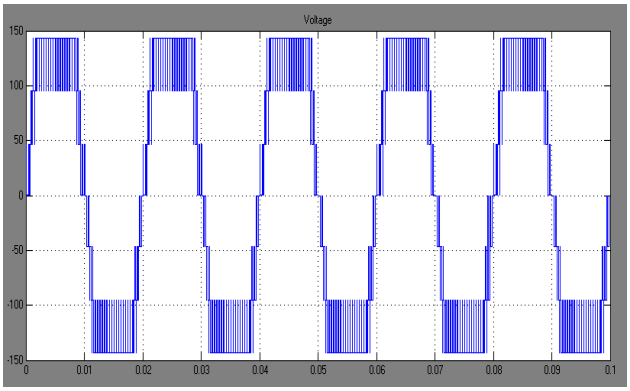


Fig: 11 Seven level output for SVPWM

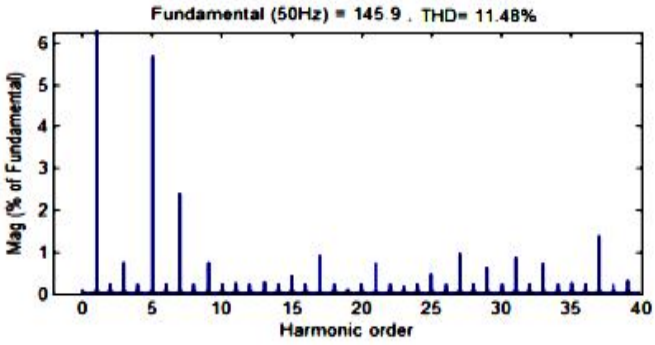


Fig: 12 FFT Analysis for SVPWM

VII. HARDWARE IMPLEMENTATION

In the hardware implementation of seven level inverter IRF840 MOSFET is used .Simple driver circuits are needed for IRF840 MOSFET. From the microcontroller, gate driver circuit for boosting the pulses is obtained. For the generation of multiple sinusoidal pulses and space vector pulses, programs are written by using PIC16F877A. The power quality analyzer analyzes the THD value and the value is 17.04% for SVPWM and 25.06% for MSPWM.

Fig: 13 Hardware Setup for SVPWM based seven level inverter

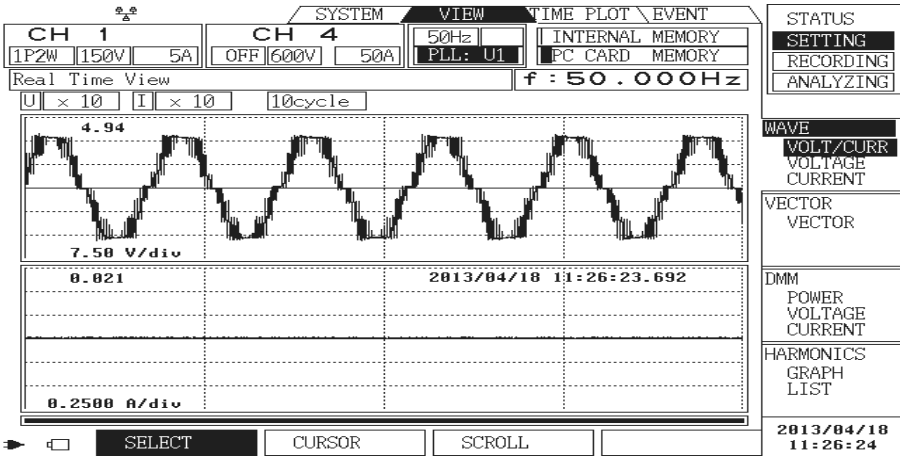


Fig: 14 Seven level output waveform of SVPWM by using Power Quality Analyzer

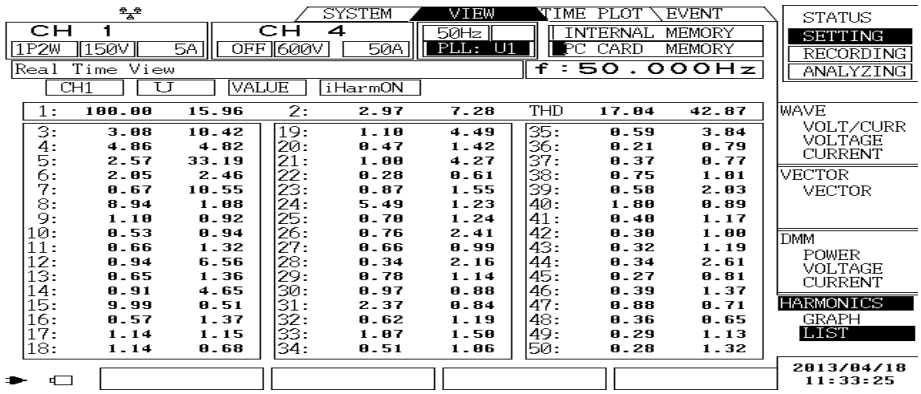


Fig: 15 THD measured by using Power Quality Analyzer

VII .CONCLUSION

This paper analyzed the PWM technique for 7 level inverter with two different PWM signals (sine and space vector). The value of THD during hardware implementation is slightly higher than that of simulation results due to the switching losses. The THD has been reduced by this control technique and without filter the output is obtained which is similar to sinusoidal waveform. The cost and switching losses are reduced by the modified cascaded multilevel inverter.

Table 3 Comparison between SVPWM and MSPWM

Modulation Techniques	Total Harmonic Distortion Analysis	
	Simulation	Hardware
SVPWM	11.43%	17.04%
MSPWM	18.63%	25.06%

Among the two modulation strategies, the THD of SVPWM technique is lower than MSPWM technique as shown in table 3.

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