IMPLEMENTATION OF A NOVEL TRANSFORMERLESS INVERTER TOPOLOGY FOR PV APPLICATION

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Abstract - Transformerless inverters are high efficiency inverters featuring high efficiency and lower size and weight. In this paper a topology based on H-bridge with ac decoupling scheme consisting of diode bridge and a switch with clamping to the DC midpoint is implemented. A 16V prototype of HB-ZVR inverter has been implemented in hardware using open loop control. The control pulses were generated using PIC18F45K22 micro-controller.

Keywords – Transformerles inverter; AC decoupling; H-bridge; Photovoltaics

I. INTRODUCTION

Two main topologies used for grid-connected PV systems are those with and without galvanic isolation. Galvanic isolation can be on the dc side in the form of a high frequency dc-dc transformer or on the grid side in the form of a low frequency but big bulky ac transformer[1].

When galvanic isolation is used the safety of the system is increased, but overall efficiency is reduced due to power losses in additional components[2]. When galvanic isolation is excluded, efficiency of the system increases as well as size and weight reduces. But its absence, may cause voltage fluctuation between the solar panel and the ground. When energized by a fluctuating voltage, leakage current flows through the stray capacitance to ground. A person, in contact with the ground and touching the PV panel, may conduct the capacitive current to the ground, causing an electrical shock. Now, this fluctuation in potential and leakage current flow depends on the inverter topology and modulation scheme chosen[3].

In order to minimize the leakage current[4] through the parasitic capacitance of the PV array and improve the efficiency, several techniques have been used[5],[6]. One method is to use Half-bridge or Neutral point clamped (NPC) topology[7] where in the midpoint of the dc-link capacitors is connected to the grid neutral. These topologies depict very high efficiencies. But its disadvantage is requirement for a high input-voltage level or else a boost stage. Another method is to separate the PV panel[11][13] from the grid for H-bridge inverters, when zero voltage is applied to the grid[12]. The separation can be on either on dc side of the inverter or its ac side. Example for dc decoupling schemes are like the H5 topology[8],[9] and ac decoupling scheme is like Highly Efficient and Reliable Inverter Concept (HERIC) topology[10].

This paper presents the implementation of a topology called HB zero-voltage state rectifier (HB-ZVR)[1][2] where the dc link midpoint is clamped to the inverter during the zero voltage period using an ac decoupling scheme consisting of a diode bridge and a switch. A 16V prototype of the topology is implemented in hardware using open loop control. The control pulses were generated using PIC18F45K22 micro- controller.

II. HB-ZVR TOPOLGY

HB-ZVR means H-bridge Zero Voltage state Rectifier topology. Generation of the zero voltage state can be done using a bidirectional switch made of one IGBT and one diode rectifier bridge as shown in Fig.1.

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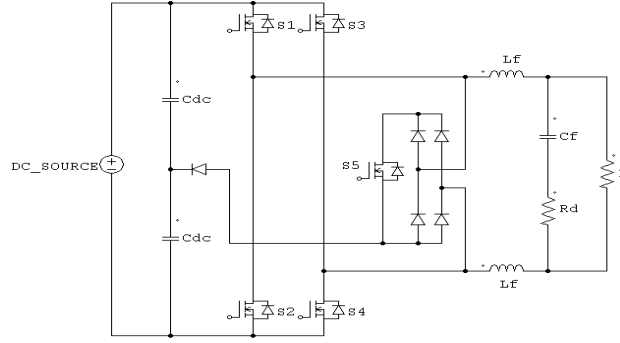
Fig.1. HB-ZVR Inverter Topology

This bidirectional switch is clamped to the midpoint of the DC-link capacitors in order to fix the potential of the PV array also during the zero voltage period, when S1-S4 and S2-S3 are open. An extra diode is used to protect the lower DC-link capacitor from short-circuiting.During the positive half wave, S1 and S4 conducts to supply positive voltage to load. When S1 and S4 are turned off, S5 is turned on to achieve zero voltage state. The signal for S5 will be the complementary gate signal of S1 and S4. A small deadtime is given in between to avoid short circuit of the input capacitor.During negative half wave S2 and S3 supply voltage to load. When S2 and S3 are turned off, S5 is turned on to achieve zero voltage state by short circuiting the outputs of the inverter and clamping it to the midpoint of the dc-link. The signal for S5 will be the complementary gate signal of S2 and S3.

III. CIRCUIT DESIGN

A. *DC-Link Capacitor*

The electrolytic DC link capacitance is used for power decoupling between the PV panel and the grid. The power into the DC link is considered as constant.

$$C_{dc} = \frac{P_{dc}}{2\omega \cdot \tilde{v_{dc}} \cdot V_{dc}} \qquad (1)$$

where P_{dc} is the average power in DC link, , ω is the grid frequency in rad/sec, $\tilde{v_{dc}}$ is the amplitude of ripple voltage, V_{dc} is the average DC link voltage.

B. *Filter Inductor*

The required inductance value is calculated by considering the moment when the ripple in the output current reaches the maximum value. Then a limit for the ripple in the output current is chosen.

$$L_f = \frac{V_{out} \cdot \Delta I_{factor}}{f_{sw} \cdot \Delta I_L} \qquad (2)$$

where V_{out} is the output voltage,ΔI_{factor} is the ripple facor, f_{sw} is the switching frequency which is chosen to be 10 KHz, ΔI_L is the limit for ripple in the output current which is chosen to be 5%.

C. *Filter Capacitor*

The output capacitor can afterward be calculated by selecting a cutoff frequency.

$$C_f = \frac{1}{4\pi^2 \cdot f_c^2 \cdot L_f} \qquad (3)$$

where f_c is the cutoff frequency and L_f is the filter inductor. The cut-off frequency of the filter must be minimally 10 times greater than grid frequency and simultaneously maximally one half of the converter switching frequency.

D.   Damping Resistor

Depending on the local-grid characteristic, a damping resistor shall be used in order to avoid possible resonance with the grid impedance.

$$R_d = \frac{1}{3. \, \omega_c \, . \, C_f} \qquad\qquad (4)$$

where ω_c is the cutoff frequency in rad/sec and C_f is the filter capacitor

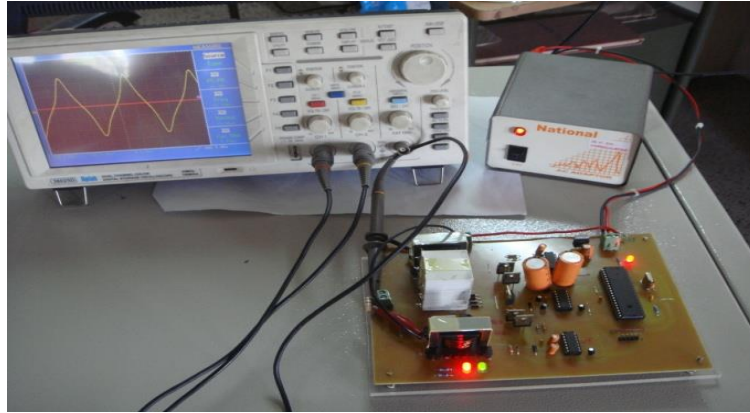## IV. HARDWARE IMPLEMENTATION

Fig.2. Hardware Setup

The power circuit of HB-ZVR inverter is implemented using IRF540N N-channel Power MOSFETs from International Rectifier and 1N5819 Schottky diodes are used in the inverter circuit. The DC-link capacitors used are electrolytic in nature. Ferrite ETD core inductors and non-electrolytic capacitors are used in the filter circuit. The hardware setup is shown in Fig.2

TABLE I - CIRCUIT PARAMETERS

Parameter	Value
Input dc voltage, V_{dc}	16V
Filter inductance, L_f	16mH
Filter capacitance, C_f	8.1µF
Load resistance, R	330Ω
Damping resistance, R_d	22Ω
DC- link capacitance, C_{dc}	4700µF
Cutoff frequency, f_c	500Hz
Switching frequency, f_{sw}	10KHz

This   hardware

implementation uses 1R2110, High & Low side Driver IC from International Rectifier for driving the IRF540

MOSFETS used in the inverter circuit. The IR2110 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. PIC18F45K22, a 40-pin, Low power, High performance micro-controller with XLP Technology is used for implementing the control circuit.

It contains two Capture /Compare /PWM (CCP) modules and three Enhanced CCP (ECCP) modules The Capture/ Compare /PWM module is a peripheral which allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals.
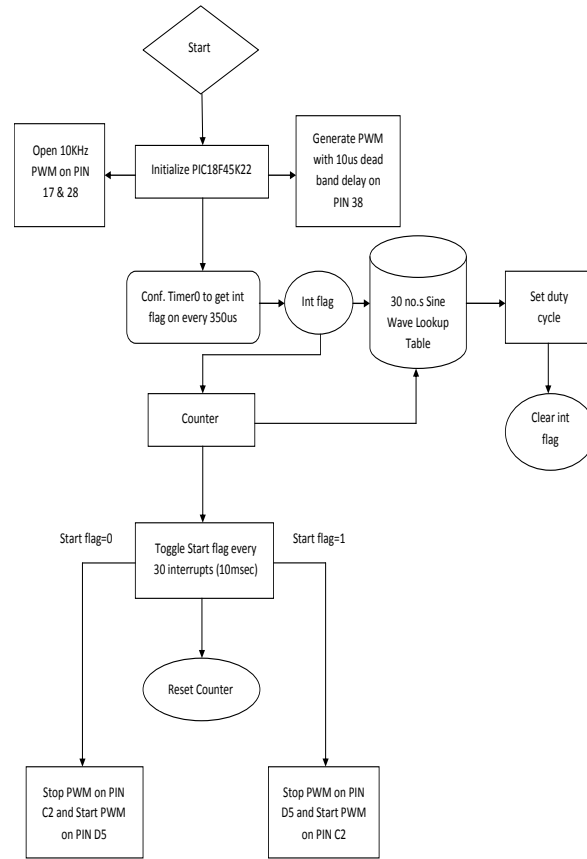

Fig.3. Flowchart for Control pulse Generation

Here PIN 17 is used to generate control pulses for MOSFETs S1 & S4, PIN 28 to generate control pulses for MOSFETs S2 & S3 and PIN 16 to generate control pulse for MOSFET S5. In order to program the PIC18F45K22 for generating the pulses for the five MOSFETs, HI-TECH C Language which runs on MPLAB editor has been used. The flowchart for generation of control pulses using PIC18F45K22 is shown in Fig.3. Fig 4 and Fig. 5 depicts the pulses given to the inverter switches. The output waveform obtained is as shown in Fig.6.
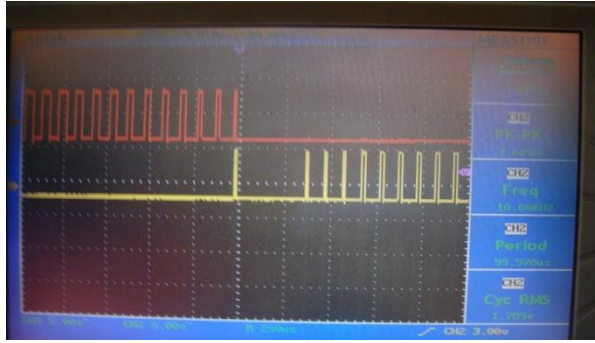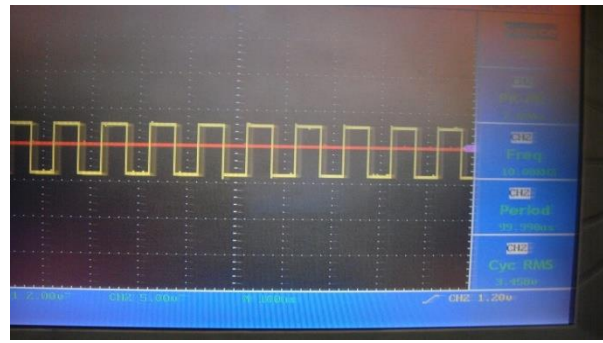
Fig.4. Pulses to H-bridge switches

Fig.5. Pulse to Decoupling Switch

The pulses given to the H-bridge switches were sinusoidal pulse width modulated at 10KHz. The decoupling switch S5 was given pulse width modulated pulses at 10KHz with a dead-time of 10µs. The inverter output waveform can be made pure sine wave by applying sinusoidal pulse width modulation to switch S5 also.
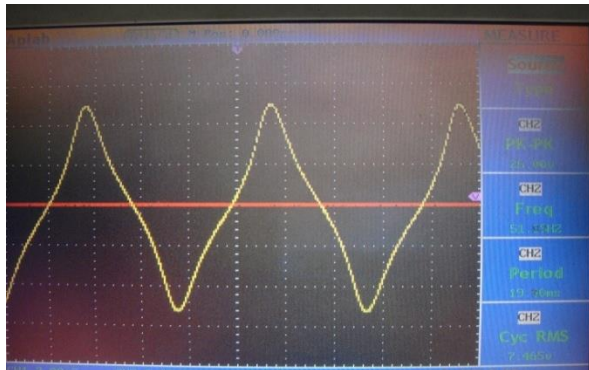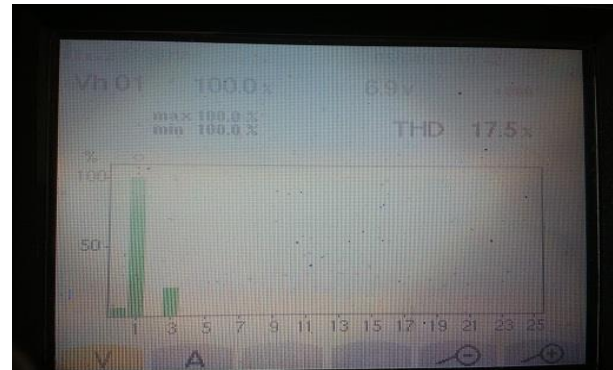

Fig.6. Output Waveform Obtained

Fig.7. THD Analysis Result

THD analysis of HB-ZVR inverter was performed using Harmonic Analyser. A THD of 17.5% with a dc component, presence of 3rd harmonic & no other higher order harmonics were observed. Fig. 7 shows the THD analysis.

V. CONCLUSION

A new transformerless inverter topology HB-ZVR (H-bridge Zero Voltage state Rectifier) has been implemented in hardware using PIC18F45K22. It has been tested for an input voltage of 16V to obtain a filtered output voltage of 13V peak. By improving the switching pulses to S5 (by making it sinusoidal pulse width modulated) better results can be obtained. THD measurement was done to obtain 17.5%. It was observed that a small DC component and 3rd harmonics were present. No other higher order harmonics were present. The hardware shows smaller size and weight suitable for a grid connected inverter and also lower cost. The most widely used topology till date is HERIC topology. HB-ZVR topology aims at reduction in number of switches compared to HERIC.

In addition it does not matter what the sign the load current has, it will always find a path through the bidirectional switch, made up of a diode bridge and a switch. This makes it possible to have a reactive power flow that can be used to support the utility grid with additional services any time during the functioning of the inverter. It is also

expected that this topology does not generate a varying common-mode voltage as the bidirectional switch is clamped to the midpoint of DC link capacitor.

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