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DESIGN OF A LOW POWER AND HIGH SPEED MULTIPLIER

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Abstract- This paper is based on multiplier structure that has a lower power consumption as well as high speed compared with the conventional one. The reduction in power is achieved by applying Pass Transistor Logic (PTL) in Conventional Full Adder to improve the efficiency of the conventional multiplier structure. In this the full adder used in multiplier is replaced by a full adder using pass transistor Logic. The simulation of this multiplier is done using TANNER EDA. Finally, a low power and high speed proposed structure is implemented, which lowers the power consumption without considerably impacting the speed. The proposed structure is assessed by comparing their speed, power, and delay parameters with those of other existing multiplier using a 45-nm CMOS technology for a wide range of supply voltages.

Keywords – Multiplier, Pass Transistor logic

I. INTRODUCTION

There is a rising requirement for low power VLSI which can be addressed at various design levels, such as the architecture, circuit, and the process technology. In the circuit level, the option for the saving of power do exists as a result of proper choice of a logic style for applying the combinational circuits.[1]This is due to all the factors which are controlling the power utilization, switching capacitance, and short-circuit currents are strongly determined by the preferred logic style. Depending on the application, the circuit to be implemented, and the technique used for design, several performance aspects become important, disallowing the configuration of universal rules for best logic styles[2].

A multiplier is one of the key blocks in most of the digital signal processing (DSP) systems. The diverse DSP applications where a multiplier plays a crucial role consist of digital filtering, digital communications and several more[3]. Computational performance of a DSP system is limited by its multiplication performance and since, multiplication dominates the execution time of most DSP algorithms, and therefore high-speed multiplier is much desired [4]. With an ever-increasing quest for greater computing power on battery operated mobile devices, design emphasis has shifted from optimizing usual delay time, area size to minimizing power dissipation while still maintaining the high performance. Hence designing of multipliers that offer any of the following design targets – high speed, low power consumption, less area or even a combination of them is of great interest[5].

II.CONVENTIONAL ARRAY MULTIPLIER

The conventional 4x4 array multiplier consists of 8-transitor(8-T) Full Adder, 5-transistor(5-T) Half Adder and 2-transistor(2-T) And gate.[6] The basic circuit layout of conventional Full adder (4 bit) is shown in Fig.1 and the schematic diagram of the multilpier is shown in Fig.2

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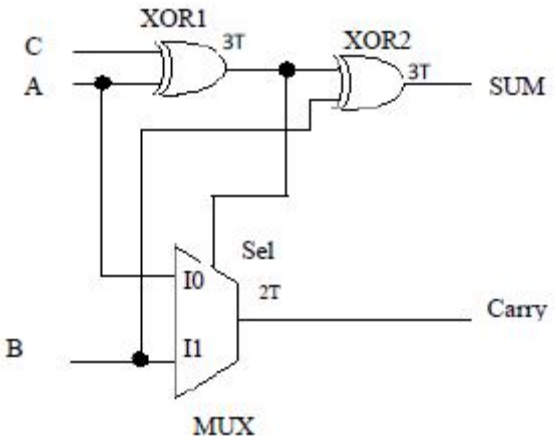

Figure 1. Conventional Full Adder

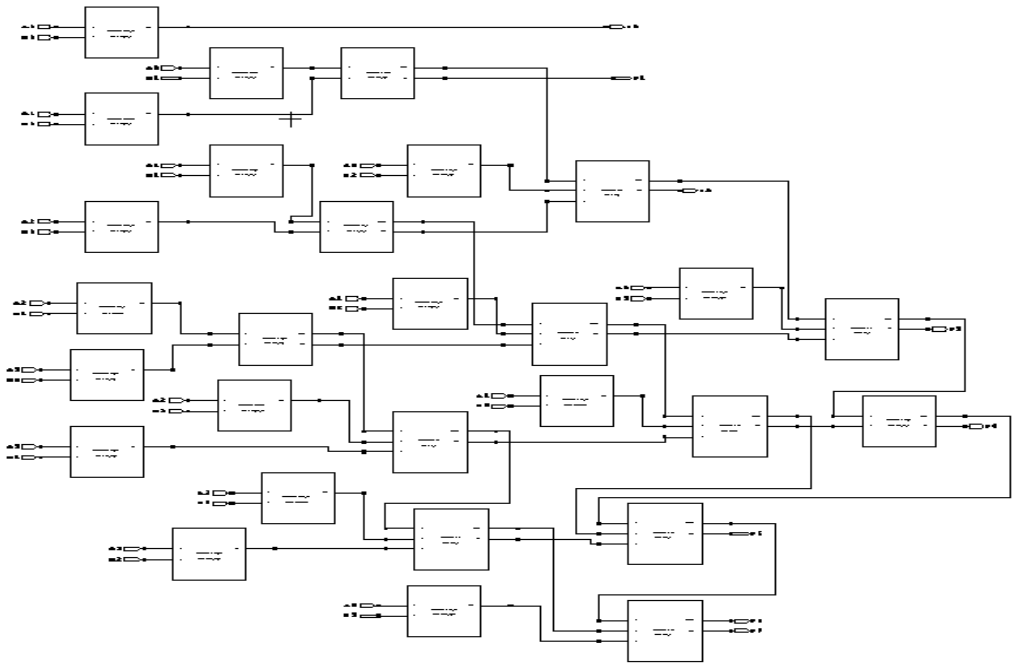

Figure 2. Schematic of Conventional Multiplier

III. PROPOSED ARRAY MULTIPLIER USING PASS TRANSISTOR LOGIC BASED FULL ADDER

In Proposed Array Multiplier, the Full Adder is based on Pass transistor Logic for better operational characteristics of high speed and low delay (shown in Fig.3) and the schematic diagram of the Pass Transistor Logic based full adder used in proposed multiplier is shown in Fig.4.[7]Subsequently, the number of transistors are reduced in the Full Adder of the proposed multiplier . Since the number of transistors is reduced in the multiplier, it results in reduced area as well as delay.

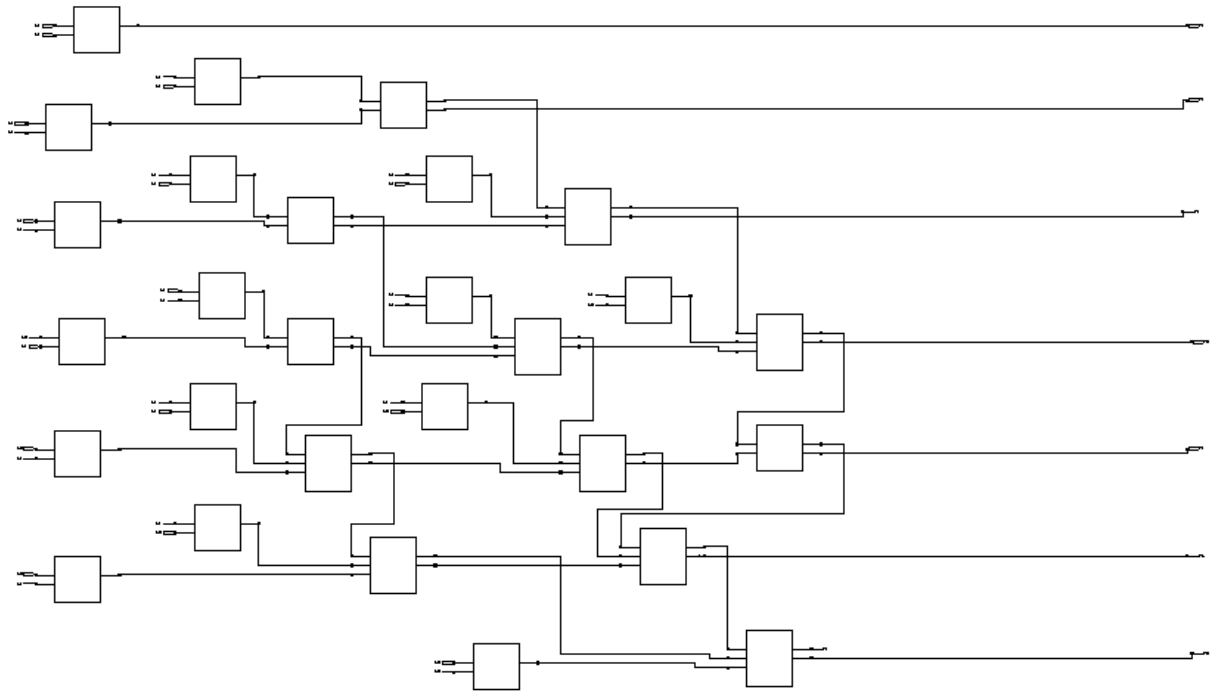

Figure 3. Proposed Multiplier using Pass transistor logic based Full Adder

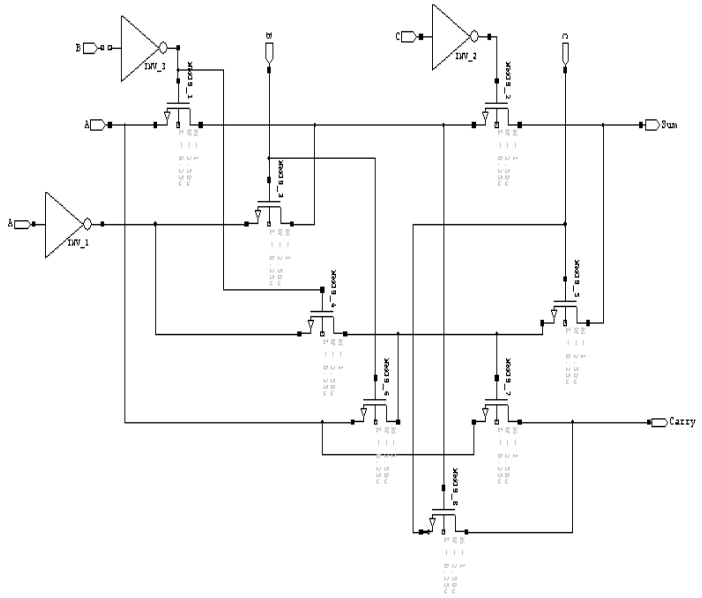

Figure 4. Pass transistor Logic Based Full Adder

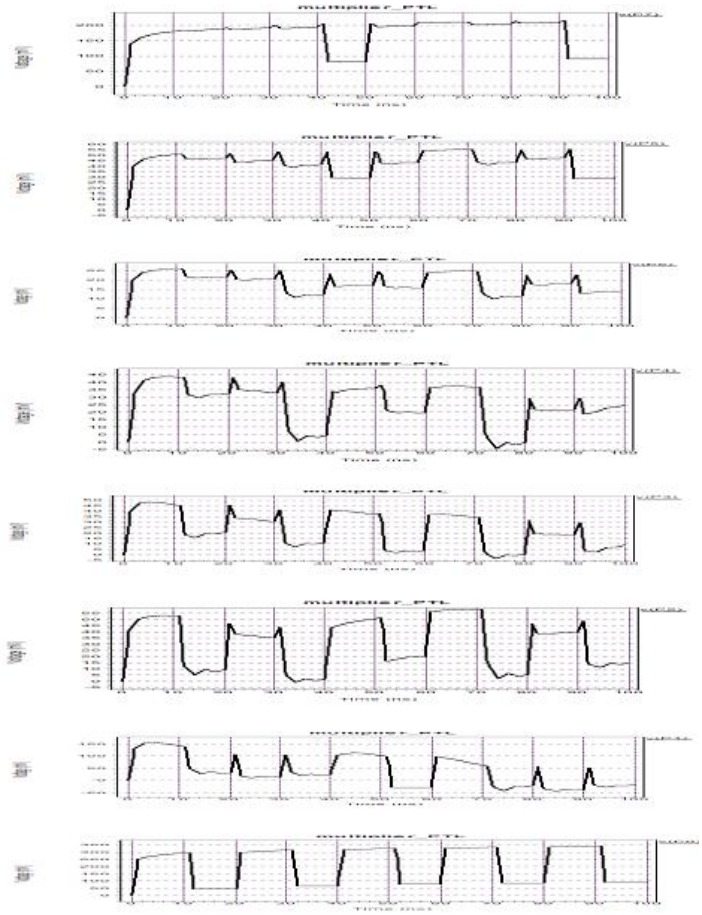

Figure 5. Output Waveform

IV.SIMULATION AND COMPARISON OF EXISTING MULTIPLIER AND PROPOSED MULTIPLIER

1. The graphs shown in Fig.6 and 7 depicts that the proposed Multiplier has better performance in comparison to the existing design [8].

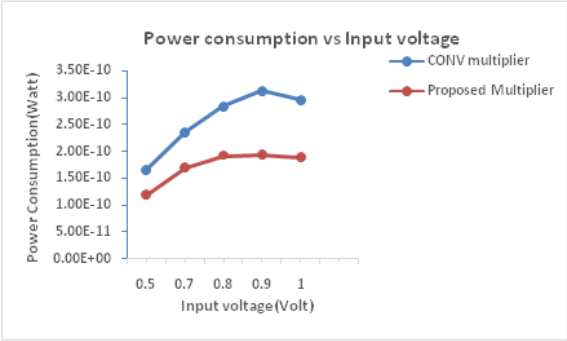

Figure 6. Power consumption with varying input Voltage

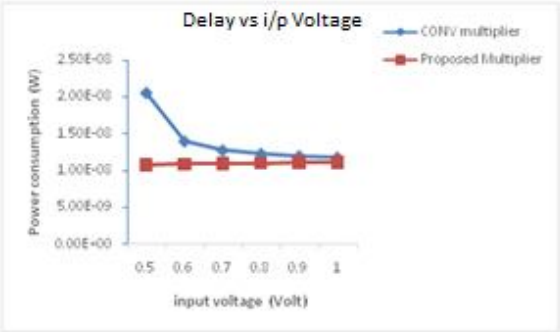

Figure.7 Delay with varying input Voltage

It was found that proposed multiplier has 30-45% and 13-35% improvement in terms of power consumption and Delay with varying input voltage as compared to the existing multiplier respectively.

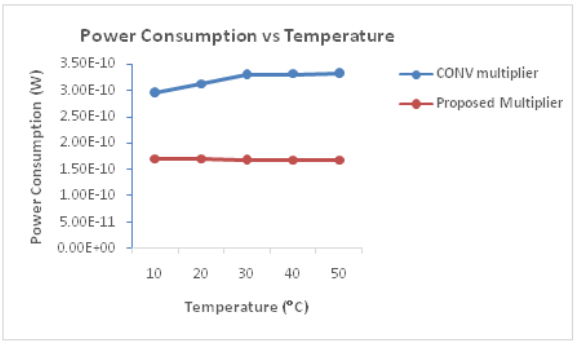

Figure 8. Power Consumption varying temperature

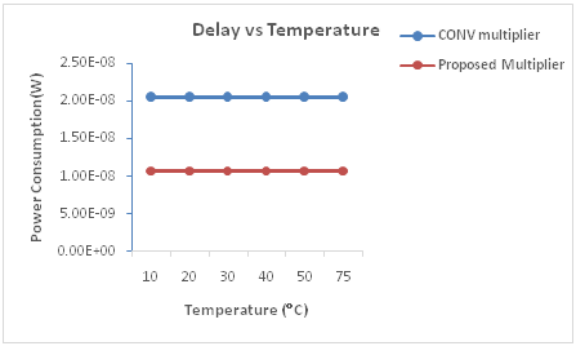

Fig.ure 9. Delay varying temperature

2. Fig.8 and 9 shows the proposed design has 63-70% and 23-45% improvement in power consumption and delay with varying temperature in comparison to the existing design Thus, the proposed design is efficient in power consumption at various system temperature as seen above.

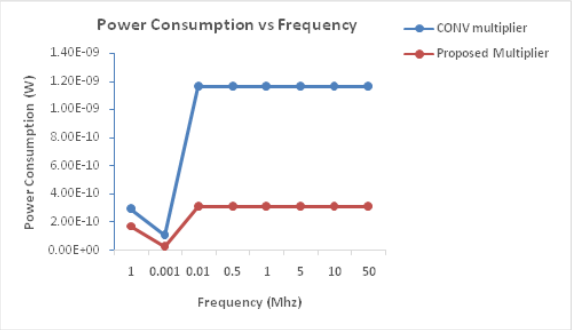

Figure 10. Power Consumption Varying Frequency

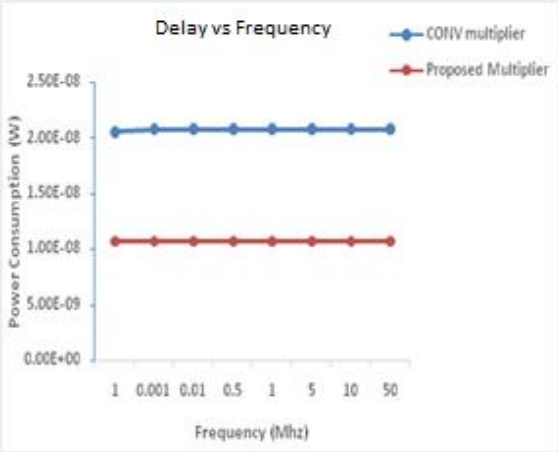

Figure 11. Delay Varying Frequency

3. Comparison in terms of power consumption and delay with varying frequency is shown in fig. 10 and 11 which illustrates that the proposed design has a lesser power consumption and delay as compared to the conventional one[9].

V.CONCLUSION

The synthesis result confirms that the proposed multiplier is suitable for low power and small area applications[10]. The Speed enhancement and lower power consumption was achieved by replacing the conventional full adder with the Pass Transistor Logic based Full Adder. The proposed circuit has been tested to have better temperature sustainability and significantly less power consumption. Again, the suggested structure showed the lowest delay and making itself as a better candidate for high-speed low-power applications.

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