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A NOVEL ADVANCED DOUBLE SWITCHING SVPWM (ADSPWM) TECHNIQUE FOR TWO LEVEL INVERTER

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Abstract- The paper proposes a novel SVPWM technique involving double switching of a phase in the sampling period of the reference vector. The work identifies all possible switching sequences, which result in same average switching frequency as conventional space vector PWM (CSVPWM). The switching sequences are arranged to clamp a phase when the current waveform at its peak value. The proposed Advanced Double switching PWM (ADSPWM) reduces the switching loss and current ripple in motor drives, compared to the existing bus clamped PWM. An insulated gate bipolar transistor (IGBT) based 2 KVA voltage source inverter (VSI) with DC bus voltage of 400 V is designed and implemented with an 8-bit PIC microcontroller (PIC18F452). The superior switching loss characteristics of the ADSPWM technique over the existing SVPWM is experimentally verified on a 415V, 2hp induction motor drive.

Keywords-Space vector, pulse width modulation (PWM), induction motor drives, harmonic distortion, switching loss.

I. INTRODUCTION

Several pulse width modulation (PWM) techniques have been reported for voltage source inverter (VSI) fed motor drives. Two popular methods to generate real-time PWM modulation are triangle Comparison method and Space Vector (SV) method. The space vector method operates in a complex plane which is divided in to six sectors of 60^0 each. Each sector is separated by eight switching state vectors as shown in Fig 1.

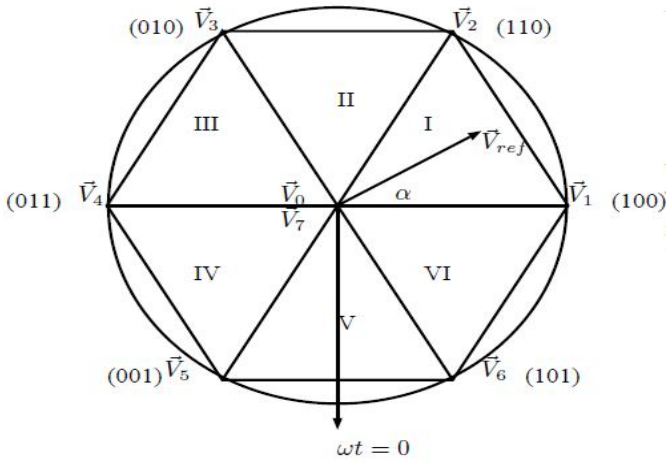

Fig. 1: Space vector diagram of three phase two level inverter

Conventional space vector PWM (CSVPWM) and third harmonic injection PWM (THIPWM) lead to higher DC bus voltage compared to sine PWM (SPWM). These techniques also result in lesser harmonic distortion in motor currents than SPWM. The division of zero vector time between the two zero states provide additional

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degree of freedom in space vector method in comparison with Triangle Comparison method [1], [2]. There are different switching sequences that have been realized to implement SVPWM [3], [4]. The flexibility in the placement of zero space-vector results in either continuous or discontinuous SVPWM (BUS clamped PWM). Discontinuous PWM techniques lead to reduction in distortion at higher line voltage over CSVPWM for a given average switching frequency. Bus clamped PWM (BCPWM) or discontinuous PWM is broadly classified into continual clamp PWM (CCPWM) and split clamp PWM (SCPWM). A phase is continuously clamped for 60^0 in a half cycle is known as 60^0 clamp PWM. In split clamp PWM, a phase clamped for γ (is known as reference angle) duration in first quarter cycle and 60^0-γ duration for second quarter cycle. If γ is 30^0, the PWM technique is known as 30^0 clamp PWM [5] − [10].

The performance of different SVPWM techniques are mainly determined by the total harmonic distortion factor of the no load current (ITHD) and switching loss. The harmonic distortion in the current is determined by the switching frequency and PWM technique employed. To reduce the filtering requirement in almost all the inverter topologies, switching frequency is increased which in turn increases the switching losses thus reducing the system efficiency. The switching frequency cannot be increased beyond a certain range due to practical limitations. The harmonic distortion in the motor phase currents must be low for satisfactory operation of the motor drive [11] − [15]. Conventional space vector (SVPWM) and other PWM techniques just sacrifices switching losses to improve the harmonic profile of the output voltage. This paper presents a novel SVPWM technique to reduce the switching loss in the medium and high power factor operation of the motor drive.

Section II of this paper analyses presents the analysis switching sequences. Section III explains the proposed advanced SVPWM technique. Section IV presents the performance analysis of the proposed advanced SVPWM techniques with respect to existing SVPWM techniques for two level inverter. The conclusions are presented in Section V.

II. MOTIVATION

In the SVPWM technique, the reference voltage is provided by a revolving reference vector which is sampled once in every subcycle Ts.

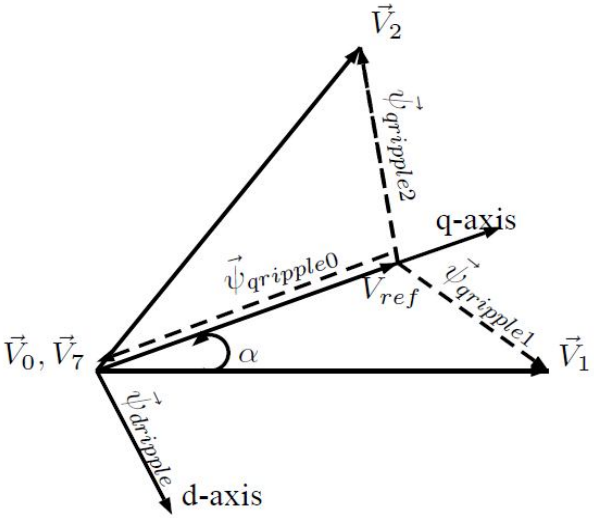


Fig. 2: Representation of flux ripple corresponding to $\vec{V}_{ref}$ in sector I

The reference vector is realized by the nearest four space vectors as shown in Fig.2 based on volt – second balance principle.

$$\vec{V}_{ref}T_s = \vec{V}_1T_1 + \vec{V}_2T_2 + \vec{V}_0T_0$$

$$T_s = T_1 + T_2 + T_0 \quad (1)$$

where $\vec{V}_{ref}$ is the reference vector , T_s is the sampling period. T_1 and T_2 are the dwell time of active vectors $\vec{V}_1$ and $\vec{V}_2$ respectively. T_0 is the total dwell time of zero vectors $\vec{V}_0$ and $\vec{V}_7$.

The dwell times T_1, T_2 , and T_0 are defined as

$$T_1 = mi\frac{\sin(60-\alpha)}{sin60}\,Ts$$

$$T_2 = mi\frac{\sin(\alpha)}{sin60}\,Ts$$

$$T_0 = T_s - (T_1 + T_2) \quad (2)$$

where mi is the modulation index

In the space vector PWM approach, the applied voltage is not equal to the instantaneous reference voltage. The applied voltage is equal to reference voltage in an average sense over the given sampling interval. This error between two voltage is defined as error voltage. The time integral value of the error voltage produces ripple in the flux linkage of the machine (flux ripple)[4]. The RMS flux ripple causes the distortion in the line current waveform. The flux ripple can be resolved along d-axis and q-axis. The corresponding flux ripple along the d-q axis is defined as

$$\begin{aligned}\vec{\psi}_{qripple0} &= \vec{V}_{ref}T_0\\ \vec{\psi}_{qripple1} &= (V_{DC}cos\alpha - \vec{V}_{ref})T_1\\ \vec{\psi}_{qripple2} &= (V_{DC}\cos(60-\alpha) - \vec{V}_{ref})T_2\\ \vec{\psi}_{dripple} &= (V_{DC}sin\alpha)T_1\end{aligned} \quad (3)$$

The RMS flux ripple can be written as

$$\vec{\psi}_{ripple} = \sqrt{\vec{\psi}^2_{qripple} + \vec{\psi}^2_{dripple}} \quad (4)$$

Where $\vec{\psi}_{qripple} = \vec{\psi}_{qripple0} + \vec{\psi}_{qripple1} + \vec{\psi}_{qripple2}$

It is observed that the application of any active voltage vector results in variation of both the d-axis and q-axis components while the application of a zero voltage vector results only in variation of the q-axis component of the flux ripple. The current distortion for a given reference vector is strongly influenced by the switching sequences used in SVPWM technique. To reduce variation in flux and distortion in line current the error voltage should be less. Therefore switching can be selectively added to reduce current ripple only in regions, where the voltage errors are large. The limited additional switching can keep the switching loss in a permissible limit. In this paper an advanced SVPWM strategy is proposed to reduce instantaneous voltage error and switching loss.

III. PROPOSED ADVANCED DOUBLE SWITCHING SVPWM (ADSPWM) TECHNIQUE

Different switching vector sequences are used to realize the reference vector. The different combinations are conventional sequences (0127-7210), bus clamping sequences (012-210, 127-721), double switching sequences (0121-1210, 7212-2127, 1012-2101, 2721-1272) and boundary sequences (010-101). Bus clamping sequences clamp a phase to positive or negative DC bus. Double switching sequence is also known as advanced bus clamping sequence. The double switching sequence produces two more times switching in each line cycle compared with conventional sequences.

The additional switching reduces the current ripple and increases switching loss. Since the additional pulses for proposed switching sequence are added when fundamental voltage crosses zero, the corresponding additional switching loss has close relationship with the power factor. On the contrary, for the conventional SVPWM, the switching actions are symmetric for the whole line cycle. Therefore, the total switching loss should be almost constant for different power factors. The optimized output current ripple and switching loss reduction with the switching sequence has close relationship with the positions of switching vectors [15]. The proposed SVPWM

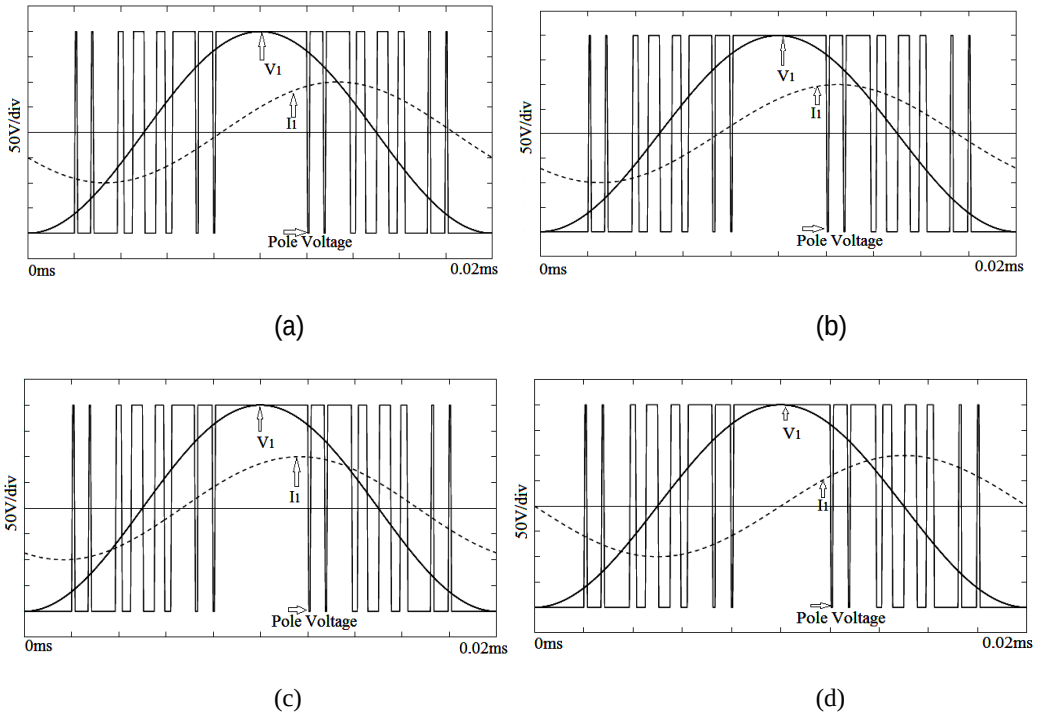
technique considers a set of sequences, and employs the best one for the given reference vector. Detailed results and analysis are presented here.

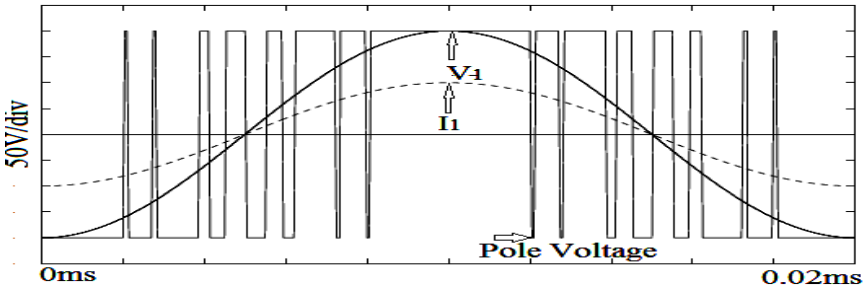
The double switching sequences are used in conjunction with conventional sequences and bus clamping sequences to design proposed advanced double switching SVPWM (ADSVPWM) technique. It is observed from Fig.1 that the current crosses zero point in the sector VI for lower power factor. Therefore it is obvious that the additional switching should be added when the fundamental current crosses zero. The load current of phase R crosses zero in sector 3 and 6 of the hexagon. Therefore the double switching sequences are arranged in such a manner that, the additional switching is applied at the current zero crossing point. R phase is clamped to positive DC rail around the peak of the current waveform (90^0). This arrangement results in reduced switching loss for medium and high power factor range (30^0–60^0). The proposed SVPWM technique maintains three phase symmetry, half wave symmetry and quarter wave symmetry.

Table I. Space vector based ADSPWM switching strategy

Sample No	Sequence used in sector I	Pulse Number
4	1272-721-210-1012	13
5	1272-2127-7210-0121-1012	15
6	1272-2127-721-210-0121- 1012	17
7	1272-2721-2127-7210- 0121-2101-1012	23
8	1272-2721-2127-721-210- 0121-2101-1012	25

Table I gives the details of ADSPWM strategy for different sample number. Consider an example of sample number 5, the sequences 1272-2127-7210-0121-1012 are used to maintain the symmetry in the three phase waveform. Active vector 1 is used in the beginning of the sector and active vector 2 is used in the ending of the sector I. Therefore active vector 2 can be used as the beginning vector of sector II. It maintains all the symmetries and reduce the complexity of the hardware. This arrangement produces a pulse number of 15.





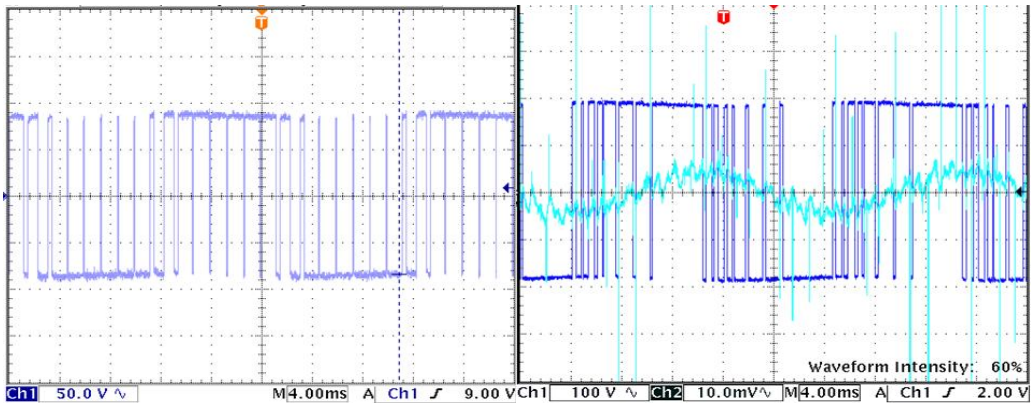
(e)

Fig. 3: variation of normalized switching losses of advanced double switching PWM at power factor angle (φ) = a) 90^0 b)60^0 c)45^0 d)30^0 e)0^0

The switching energy loss in a subcycle depends on the per phase current value and the number switchings of the phase in the given sample. The variation of switching energy loss over the fundamental cycle for ADSPWM is shown in Fig.3 for different values of the power factor angle. The fundamental voltage (V1) waveform is represented by the thick line. The dotted line shows the fundamental current (I1) waveform. The experimental verification of the proposed SVPWM technique is present in next section.

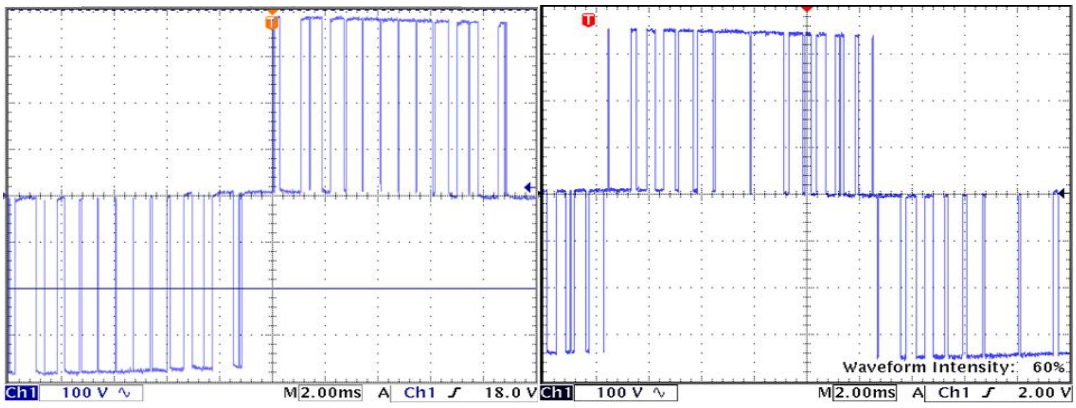
IV. EXPERIMENTAL SETUP AND PERFORMANCE EVALUATION

The experimental setup comprises of three insulated gate bipolar transistor (IGBT) power modules from SEMIKRON (SKM50GB123D) for the power stage of voltage source inverter. The strategies are designed and implemented with an 8- bit PIC microcontroller (PIC18F452).The DC voltage is 400 V, and the fundamental and switching frequencies are chosen as 50 Hz. A 415 V, 2 hp, 50 Hz, 3-phase induction motor is used to verify the different SVPWM switching strategies. Fig.4, 5 and 6 present pole voltage , line voltage and FFT spectrum of CSVPWM and ADSPWM strategy.



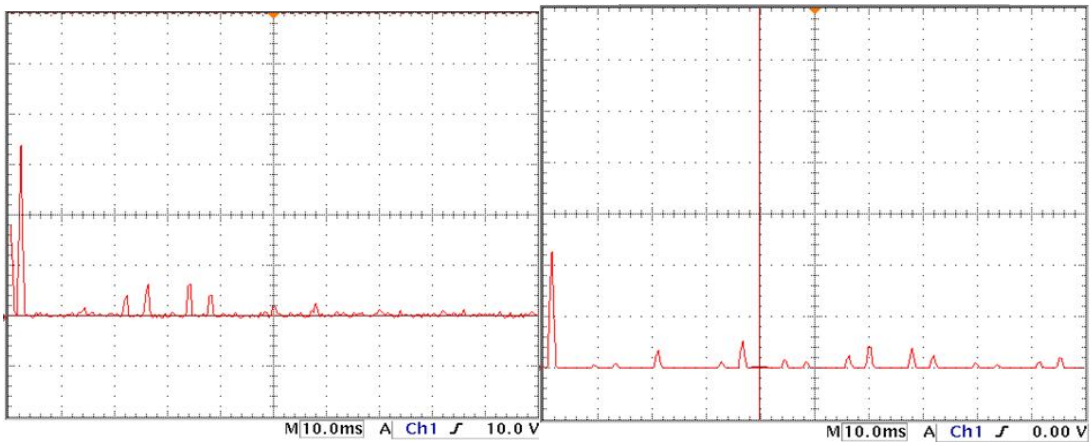
(a) (b)

Fig. 4: Pole voltage waveform of a) CSVPWM b)ADSPWM



(a) (b)

Fig. 5: Line voltage waveform of a) CSVPWM b)ADSPWM



(a) (b)

Fig. 6: FFT spectrum of a) CSVPWM b)ADSPWM

The performance matrices for different SVPWM strategies considered are weighted voltage total harmonic distortion (Vwthd) and Switching loss respectively. The weighted voltage total harmonic distortion is defined as $V_{wthd} = \frac{1}{V_1}\sqrt{\sum_{n=1}(\frac{V_n}{n})^2}$ where V_1 and V_n are the RMS values of the fundamental and n^{th} harmonic voltage of the line voltage waveform respectively. The weighted voltage THD is approximately proportional to the current THD and independent of motor parameters. The performances of different SVPWM strategies based on weighted voltage THD are calculated for the modulation index range (mi) 0.5 to 0.866.

The switching loss of a SVPWM strategy is proportional to the DC bus voltage, number of switching per phase, switching sequence used and current flowing through the device [6]. Therefore switching loss for a subcycle is depend on the number of switching per subcycle and the phase current. The switching and phase current waveform are shown in Fig4.b. It is observed that phase is clamped during the positive and negative peak of current waveform. The switching frequency is more in the zero crossing of current waveform.

V. RESULTS AND DISCUSSION

In the present implementation the fundamental frequency (50Hz) is fixed with respect to various sample number. All the strategies (CSVPWM, ASCPWM [6], ACCPWM [6]) including the proposed strategy are

compared with respect to same pulse number. Hence the performance of proposed SVPWM strategy is not affected by the increased number of switching in a sequence. The THD obtained from the experimental results are shown in Fig.7. It shows that the proposed ADSPWM strategy reduces the THD in the higher modulation index region compared to CSVPWM. The zero vector changing sample in ASCPWM and ACCPWM strategies are located at 30^0 .

Table II. SVPWM switching sequences of existing and ADSPWM in the sector I (Sample No = 5)

SVPWM Technique	Sequences used in sector I
CSVPWM	0127, 7210, 0127, 7210, 0127
ASCPWM	0121, 1210, 0127, 7212, 2127
ACCPWM	7212, 2127, 7210, 0121, 1210
ADSPWM	1272, 2127, 7210, 0121, 1012

The switching sequences used in different SVPWM techniques for sector I are summarized in Table II.

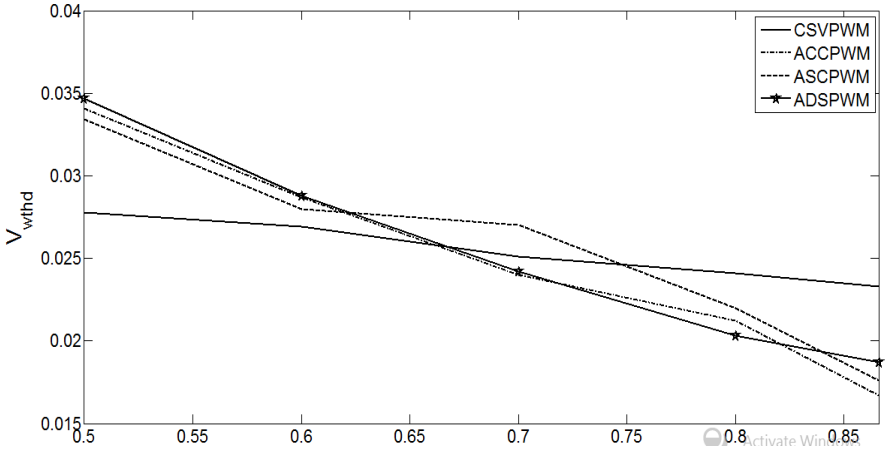


Fig. 7 Vwthd Performance assessment with pulse number 15

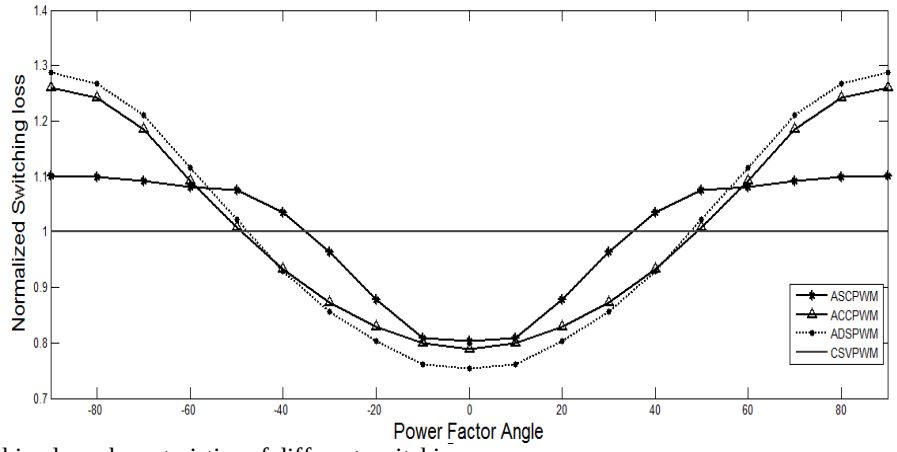


Fig.8 Switching loss characteristics of different switching sequences

The normalized switching loss characteristics of the ADSPWM and existing SVPWM techniques compared to CSVPWM is shown in Fig.8. The switching loss is less compared to CSVPWM ($-45^0$to$+45^0$) and comparable to

the existing advanced SVPWM techniques. From Table I it is clear that the additional switching is added at the zero crossing of the current waveform. This results in reduced switching loss. Fig.8 demonstrates that the ADSPWM outperforms ASCPWM for power factor angle (lagging and leading) over the range of $-45^0$to + 45^0 with respect to switching loss. ADSPWM outperforms ACCPWM over the range 30^0to90^0 for both lagging and leading power factor. ADSPWM deteriorates by 5% outside the mentioned range with ACCPWM.

Table III. The switching loss characteristics of the ADSPWM with existing advanced SVPWM

Power factor (MI = 0.8)	ACCPWM (60^0)	ASCPWM (30^0)	ADSPWM
0^0-30^0	85%	72%	75%
30^0-45^0	96%	85%	85%
45^0-60^0	107%	114%	112%
60^0-90^0	108%	131%	128%

Comparison of performance index switching loss of ADSPWM technique with advanced SVPWM [10-18] over conventional SVPWM is given in Table III. The average percentage of reduction in switching loss of ACCPWM, ASCPWM compared to CSVPWM are 15% and 28% where as the corresponding reductions in switching loss by the ADSPWM technique is 25% for unity power factor operation. It is observed that ADSPWM performs better in the $-45^0$to + 45^0 power factor range in CSVPWM.

VII. CONCLUSION

The work introduces a new SVPWM switching strategy based on double switching sequence for two level inverter. To minimize the switching loss the additional pulses in double switching sequence should add in the zero crossing of the current waveform. The reduction in switching loss is verified by experimental results. The ADSPWM strategy provides less THD compared to CSVPWM and comparable results with existing advanced SVPWM techniques in the medium power factor range.

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