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DESIGN OF VITERBI DECODER USING HYBRID REGISTER EXCHANGE METHOD FOR LOW POWER APPLICATIONS

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Abstract- With increasing demand of wireless multimedia business, it is necessary to call for strict criterion on speed and power consumption of portable devices. Viterbi Decoder serves as an important role in error correction of communication devices.Significant power reduction can be achieved by modifying the design and implementation of viterbi decoder. In this paper we proposed the methods for survivor path storage and decoding as traceback (TB) and register exchange method (REM).REM cosumes large power and area, due to huge switching activity.The problem of switching activity of Viterbi decoder can be reduced by combining TB and REM and the method called Hybrid Register Exchange Method (HREM).The Viterbi decoder is designed using REM, HREM and simulated on Xilinx tool and power is calculated on Xilinx power analyser. As the switching activity is reduced in HREM the viterbi decoder achieves reduction in power in HREM as compared with REM.

Keywords – Viterbi decoder, Traceback, REM, HREM

I. INTRODUCTI ON

The Viterbi decoder algorithm proposed in 1967 by Andrew J. Viterbi is a decoding process for convolution codes in memoryless noise. Viterbi decoder algorithm is an exact recursive algorithm for finding the shortest path through a trellis, and thus is actually an optimum trellis decoder. it is capable of handling extremely high speeds (tens of megabits). In Mobile station baseband modem [3], the Viterbi decoder consumes more than one-third of the chip area and the power dissipation of the baseband modem Therefore, a low-power implementation of the Viterbi decoder is a significant practical matter.

For viterbi decoder [10] there are two well known methods for survivor path storage and decoding, the Trace- back method (TBM) and Register Exchange method (REM). In trace-back method, memory requirement is high. TBM is the preferred method used in Viterbi decoders having large constraint length and high performance. However, the TBM has drawbacks, which requires last-in-first-out (LIFO) buffer and has to use multiple read operations for high speed operation. This multiple operation results in complex control logic. The REM is logically simple,

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but it will consume large power and area, due to huge switching activity. The problem of switching activity of viterbi decoder can be reduced by combining TB and REM that is Hybrid Register Exchange Method (HREM).

The following sections are arranged as follows .We first briefly review the Convolutional encoder with all components in sections and about the decoding methods using REM and HREM Methods.

II. CONVOLUTIONNAL ENCODER

A Viterbi decoder and Convolutional encoder operate by finding the most likely decoding sequences for an input code symbol stream. A convolutional encoder is selected for error correction with digital mobile communication. Binary convolutional encoder can be implemented using shift registers and exclusive-OR gates (modulo-2 adder)

We have designed convolutional encoder with (3, 1, 2) specification ie (n, k, m) where n is input bits of encoder, m is number of memory elements and code rate of convolutional encoder is given by k/m i.e 1/2. Convolutional encoder with two shift register and two XOR gates which produce two bits output i.e Out0 & Out1 for single bit of input.

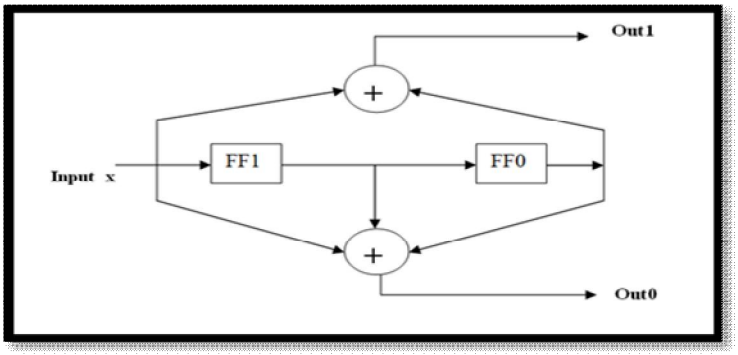


Figure 1. Block diagram of convolutional encoder K=3, k=1, n=2

Out0 = Input $\oplus$ FF1$\oplus$ FF0 (1)

Out1 = Input $\oplus$ FF0 (2)

III.VITERBI DECODER

At the destination, the decoder utilizes the trellis diagram to decode the received stream by finding the sequence with the maximum likelihood. Viterbi decoder consists [11] of three basic computation units. The branch metric Unit (BMU), the Add-Compare-Select Unit (ACSU) and the Trace Back Unit (TBU). The BMU calculates the branch metrics by Hamming distance or Euclidean distance, and the ACSU calculates a summation of the branch metric from the BMU and previous state metrics, which are called the path metrics. After this summation, the value of each state is updated and then the survivor path is chosen by comparing path metrics. The TBU processes the decisions made in BMU and ACSU, and outputs the decoded data.

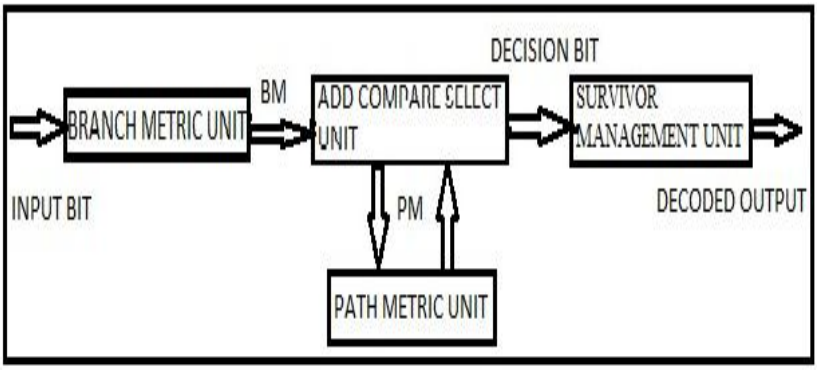


Figure 2. Viterbi Decoder

IV.REGISTER EXCHANGE METHOD

As shown in Figure3. a register is assigned to each state contains information bits for the survior path throught the trellis.The register keeps partially decoded output sequence along the path.The register exchange method eliminates the need to traceback since the register of final state contains the decoded output, but it requires the complex hardware due to the need to copy the content of all the registers from state to state.

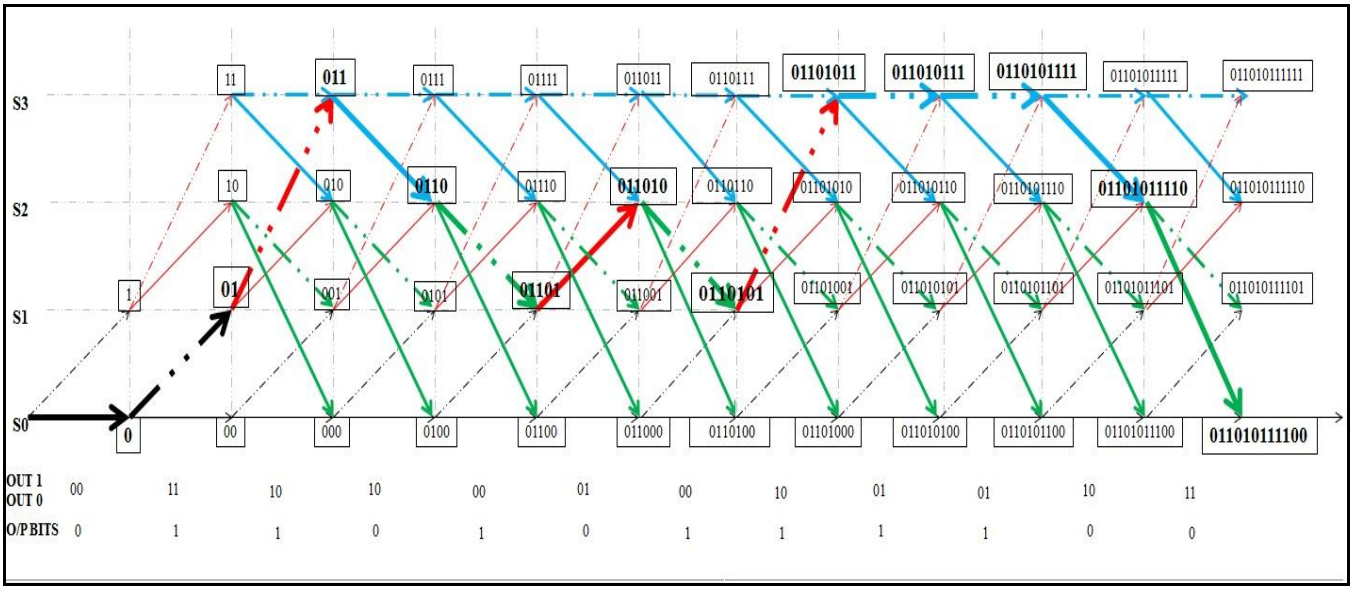
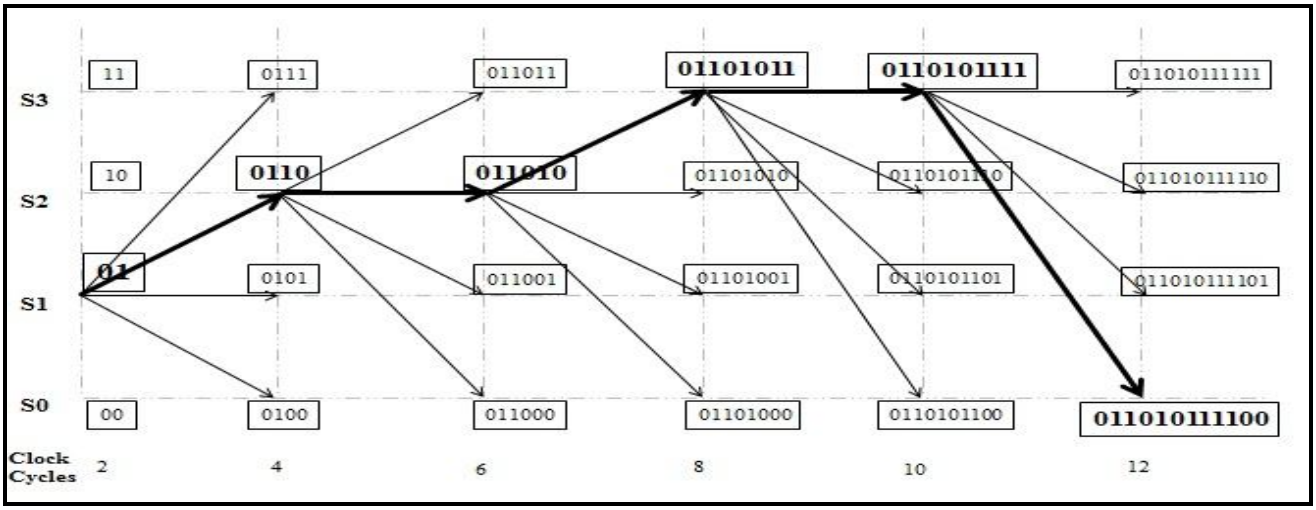


Figure 3. Register Exchange Method

V. HYBRID REGISTER EXCHANGE METHOD

Hybrid Register Exchange method is combination of register exchange method and Traceback method hence the name Hybrid register exchange method. This method reduces the switching activity and power. In HREM instead of processing single bit in a cycle, now two bits are decoded, which reduces the switching activity to half as compared to REM.In this method we are

using a property of trellis. Initial state can be first traced back through an m cycle.Then contents of initial state transfer to current state and the next m bits of the register is the m bits of current state itself as shown in fig.4 .



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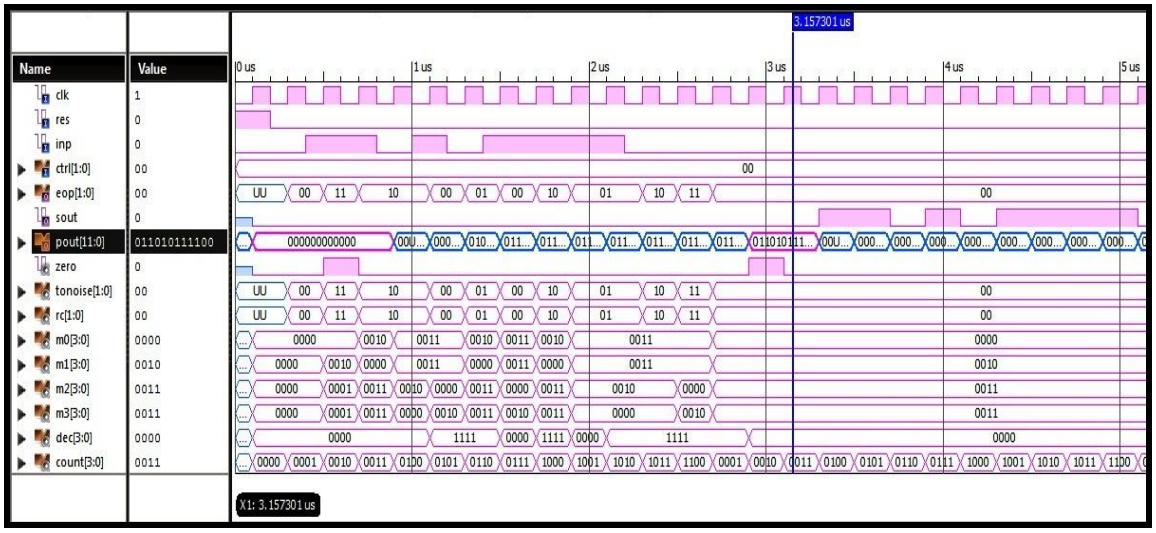
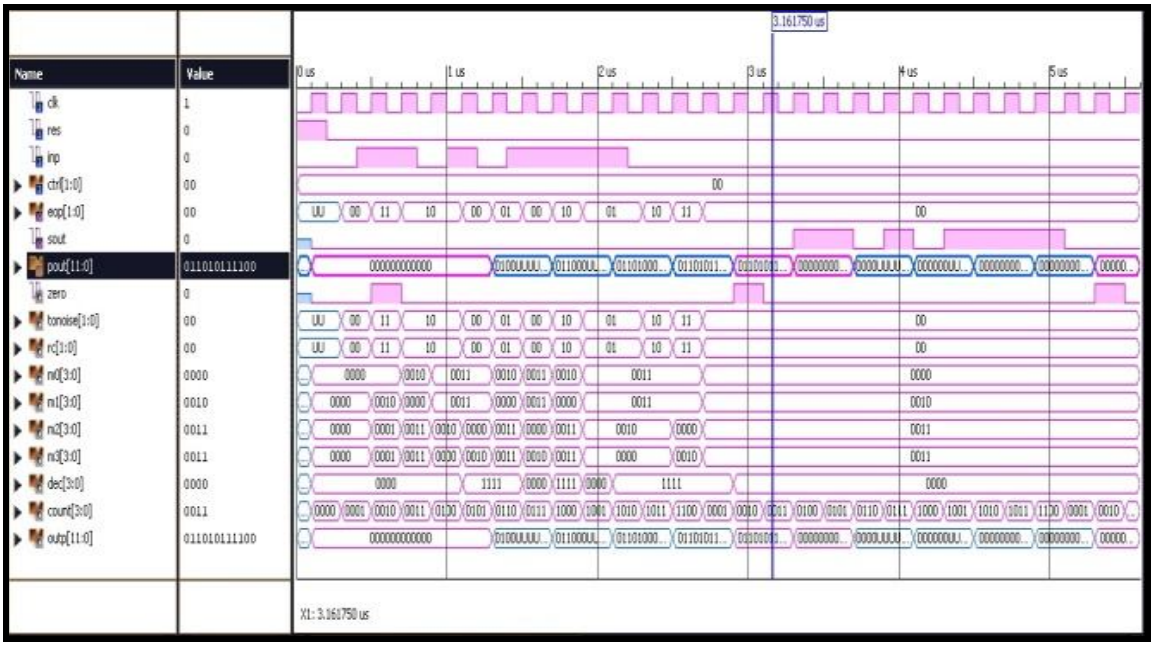
. ***Figure 4. Hybrid Register Exchange Method***

VI. SIMULATION RESULTS

The modules of viterbi decoder like ACSU and Register exchange blocks are designed and verified for various combinations



. Figure 5. Simulatin Result REM for input bit sequence 011010111100



. Figure 6. Simulation Result HREM for input bit sequence 011010111100

Table I. Result of Power Measurment

Methods	**REM**	**HREM**
Power Dissipation (Watts)	**0.035**	**0.029**

IV.CONCLUSION

In this paper we designed viterbi decoder for low power consumption using Register exchange and Hybrid register exchange method for constraint length K=3 and code rate 1/2.The design of viterbi decoder is simulated using Xilinx tool and power is analyzed using Xilinx power analyzer. For the given sequence of inputs it has been observed that the power consumption in HREM is less as compared to REM.

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