Design of Low voltage, Low Power and High Speed Logic Gates Using Modified GDI Technique

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Abstract- In low-voltage and low-power applications, optimization of several devices for speed and power is a significant issue. These issues can be overcome by incorporating Modified Gate Diffusion Input (Mod-GDI) technique. This technique has been adopted from Gate Diffusion Input (GDI). The Mod-GDI technique allows reducing power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. This paper presents the various Performance comparisons on low power techniques of different combinational logic functions and to state that the proposed Modified Gate Diffusion Input logic (Mod-GDI) to be much more power-efficient than Gate Diffusion Input logic (GDI) and static CMOS logic design with 1.8V supply voltage. By this work it is to be known that the design of different practical circuit arrangements that reveals the Mod-GDI to be superior than GDI and CMOS in the major cases with respect to supply voltage, propagation delay and total power dissipation. The designs are simulated using Mentor Graphics tools with a supply voltage of 1.8V at 90nm Process technology.

Key words—Gate Diffusion Input (GDI), Mod-GDI, Total power dissipation, Propagation delay, Low Voltage

I. INTRODUCTION

With advancements in technology and the expansion of mobile applications, power consumption is one of the fundamental limits in both high performance microprocessors and low to medium performance portable systems, has become a primary focus of attention in VLSI digital design [1-4]. In high performance systems, power is the limiting factor for a further increase in clock speed and circuit density, due to the difficulties of conveying power to circuits and removing the heat that they generate [5]. In portable battery operated devices, such as cellular phones, bio-medical devices, sensor networks, etc., power consumption is critical, since it determines the lifetime of the battery (for non-rechargeable) or the time between recharges. It also affects the device size, cost and weight.

Although Static CMOS Logic has been the most popular design approach for the past three decades, many attempts have been made to propose a better alternative to achieve lower power dissipation, smaller area and better performance. In the past, Pass-Transistor logic (PTL) was proposed as a promising alternative to Static CMOS Logic [6]-[9]. A comprehensive comparison between the PTL and Static CMOS approaches was presented by Zimmermann et al. [7]. Pass-transistor design was found to be well-suited to circuits that contain large proportions of XOR gates and multiplexers, such as arithmetic units, as PTL implementations of these functions are more efficient than conventional CMOS implementations [6] ,[8]. On the other hand, PTL implementations of logic gates such as NANDs and NORs, were found to be slower and consume more power than CMOS implementations [8], [9], mainly because of the reduced output swings due to the threshold drop across a single channel pass transistor. Moreover, the leakage of PTL implementations of monotonic gates was shown to be much higher than that of CMOS implementations [10].

The main concentration of this paper at the circuit level is to propose the logic gates (Not, AND, OR, EX-OR, NAND, NOR) and 2X1 multiplexer using the modified GDI techniques and compare the total power dissipation with respective to GDI and static CMOS techniques. Latter these power efficient logic gates can be used to design adders, Multipliers and all other digital applications.

II. MODIFIED GATE DIFFUSION INPUT(MOD-GDI)

In [10], a new low-power design technique, namely Modified Gate Diffusion Input (Mod-GDI) which is adopted from GDI technique[11].This Technique allows implementation of a wide range of combinatorial synchronous functions using only two transistors has been described. This method is found to be suitable for design of fast, low-power circuits, using minimum number of transistors (as compared to CMOS and existing PTL techniques), while simultaneously improving logic level swings and static power characteristics and allowing simple top-down design methodology by using a small cell library. Table.I illustrates the input configurations that guarantee better results for the required logic functionality using MoD-GDI technique. Unlike the basic GDI proposed in [2] where the substrate connections of NMOS and PMOS are connected to sources of the respective gates, in Mod-GDI technique the NMOS and PMOS substrate connections are connected to ground and VDD respectively. Figure1. depicts the basic Mod-GDI cell, which is unlike a conventional CMOS implementation, where the source of the PMOS and the source of the NMOS are actually fed by the value of the input signals.

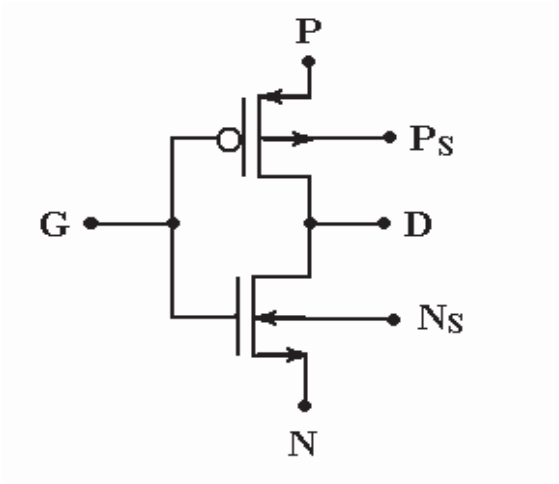

Figure1. The basic Mod-GDI cell

Table I. Input Configurations of Different Logic functions

N	NS	P	PS	G	D	Function
0	0	1	1	A	A^1	INVETER
B	0	0	1	A	AB	AND
A	0	B	1	A	A+B	OR
A^1	0	A	1	B	A^1 B+AB^1	EX-OR
A	0	A^1	1	B	AB+A^1 B^1	EX-NOR
0	0	B	B	A	A^1B	FUNCTION
C	0	B	1	A	A^1B+AC	MUX

A. Important Features of Mod-GDI Technique

The MoD-GDI logic style provides a low-power and area efficient substitute to existing logic styles, which is implementable in all current CMOS transistor fabrication technologies. Mod-GDI is appropriate for design of high-speed, low power circuits, using reduced number of transistors, even as improving swing degradation and static power characteristics, and allowing easy top-down design by using a small cell library. Mod-GDI is appropriate for implementation of a broad range of logic circuits, using a variety of transistor technologies. Mod-GDI logic style performance is testable; so that Mod-GDI logic style and logic circuit design methods is therefore a promising new approach to logic circuit design.

Realization of logic functions in Silicon-on-Insulator (SOI) or Silicon-on-Sapphire (SOS) fabrication technologies presents considerable reduction of wires used for interconnect, in these methods, the floating bulk transistors are

frequently used for logical circuit's implementations for GDI logic style and for other existing logic styles. Floating bulk transistors not requires connections of the VDD and GND wires to the transistors bulks. Consequently, when a logic function is implemented with Mod-GDI cells with SOI or SOS transistors, VDD and GND interconnect wires are not required because the Mod-GDI cell requires VDD and GND only to supply the bulks. This is in contrast to the majority previous design methodologies which would still need VDD and GND to supply the circuits.

B. Combinational Primitive Logic Gates

In digital circuit theory, combinational circuits sometimes called as time independent logic is a type of digital logic which is implemented by Boolean circuits, where the output is a pure function of the present input only. The basic logic gates like INVERTER, AND, OR, NAND, NOR , EX-OR gates are sometimes called as primitive logic gates. A logic gate is an idealized or physical device implementing a Boolean function that is, it perform a logic operation on one or more logical inputs and produces a single logical output. A large number of electronic circuits are made up of logic gates. Logic circuits include such devices as multiplexers, registers, arithmetic logic units (ALUs), and computer memory which may contain more than 100 million gates. The three types of essential logic gates are AND, OR and NOT gate. With these three any conceivable Boolean equation can be implemented. The comparison of logic gates such as AND, OR, XOR, XNOR were carried out for the Mod-GDI, standard CMOS, Transmission Gate(TG) and Differential Pass Transistor (DPL) logic style. Among all, Mod-GDI requires minimum number of transistors and reduced power consumption .Table II shows the comparison between four styles in terms of transistor count.

Table II. Comparison of Transistor Count

Functions	Mod-GDI	DPL	TG	CMOS
AND	2	7	6	6
OR	2	7	6	6
XOR	4	8	8	16
XNOR	4	8	8	16

III. PROPOSED PRIMITIVE GATES USING MOD-GDI TECHNIQUE

Figure 2 – Figure 9 represents the proposed designs of primitive gates namely Inverter, 2 input AND gate, 2 input OR gate, 2 input NAND gate, 2 input NOR gate, 2 input EX-OR gate, 2 input EX-NOR gate and 2X1 multiplexer using Modified GDI technique. All the proposed designs are design at 90nm technology with very low supply voltage of 1.8V and to get minimum area the designs are designed at W/L ratio of 6. The low power supply will obviously improves the total power dissipation of the design.

A. Inverter

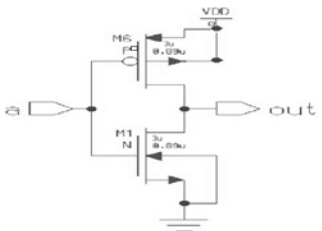

Figure 2. Inverter using Mod-GDI Technique

B. Two input AND gate

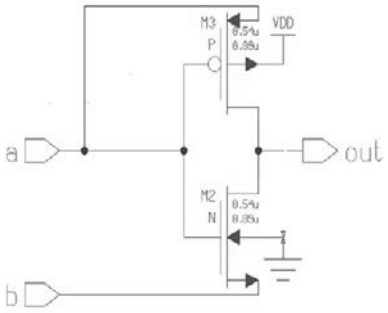

Figure 3. Two input AND gate using Mod-GDI Technique

C. *Two input OR gate*

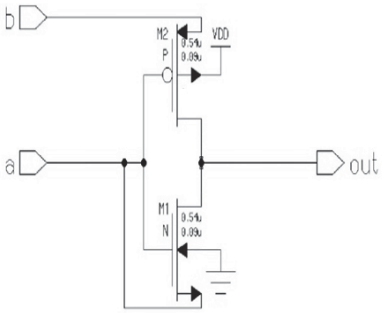

Figure 4. Two input OR gate using Mod-GDI Technique

D. *Two input NAND gate*

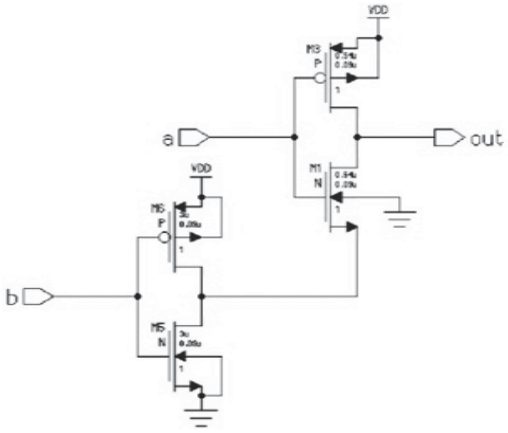

Figure 5. Two input NAND gate using Mod-GDI Technique

E. *Two input NOR gate*

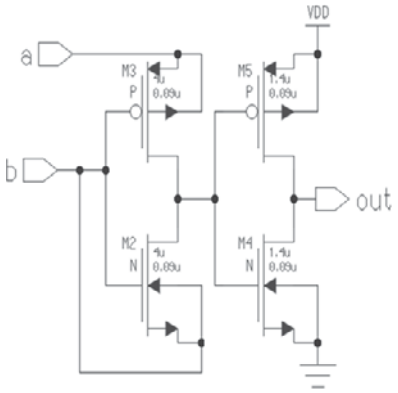

Figure 6. Two input NOR gate using Mod-GDI Technique

F. Two input EX-OR gate

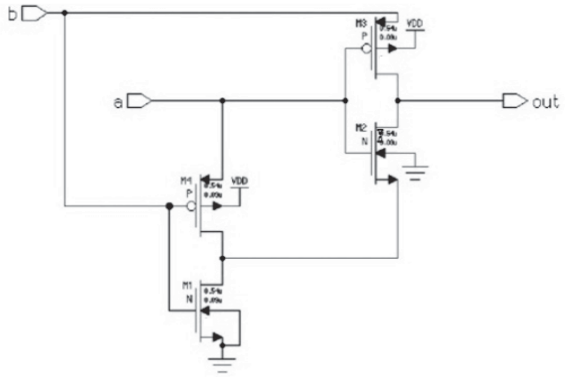

Figure 7. Two input EX-OR gate using Mod-GDI Technique

G. Two input EX-NOR gate

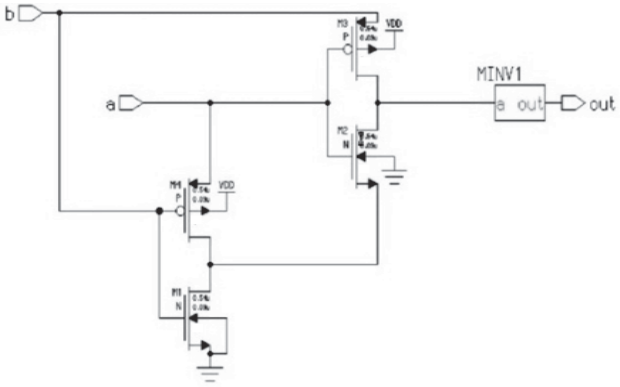

Figure 8. Two input EX-NOR gate using Mod-GDI Technique

H. 2X1 Multiplexer

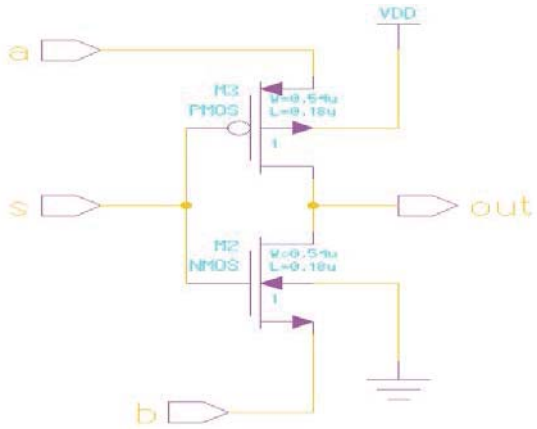

Figure 9. 2X1 Multiplexer using Mod-GDI Technique

IV. RESULTS AND ANALYSIS

Figure 10- Figure 17 gives simulation reports of the proposed logic gates using Mod-GDI technique. In the simulation results it is observed that the unwanted glitches have been obtained due to the improper input timings. Though the designs dissipate less power and outputs are at full swing than comparative to all other existing techniques. Table III showing the comparison of total power dissipation with respective to all other techniques [1].

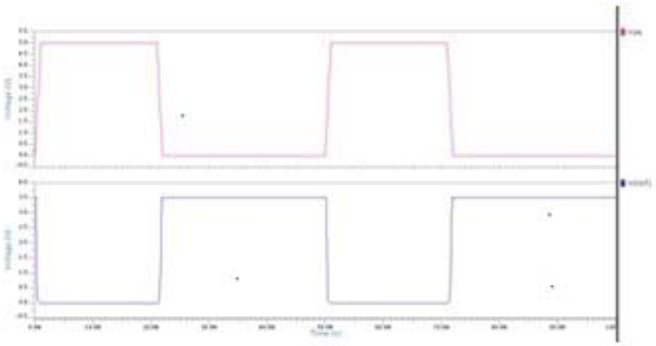

Figure 10. Simulation result of inverter

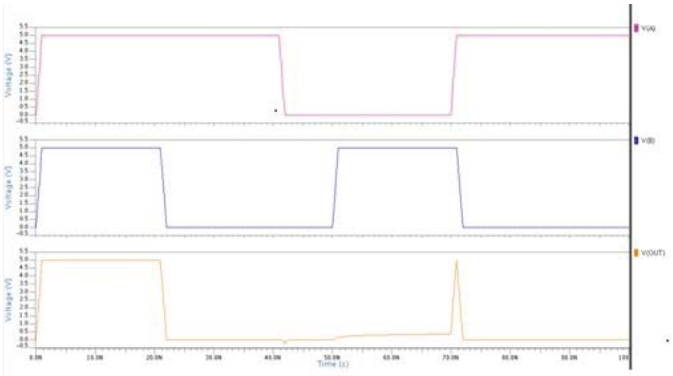

Figure 11. Simulation result of 2 input AND gate

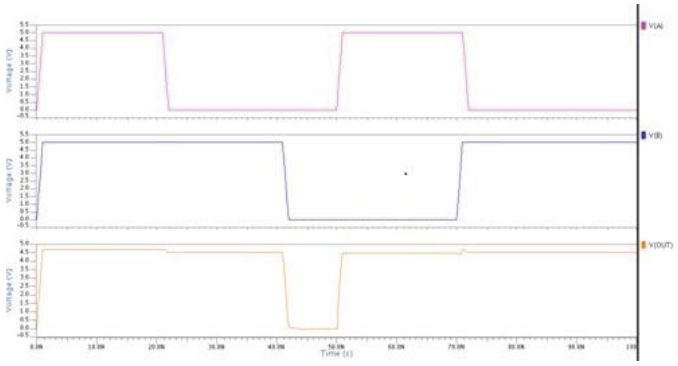

Figure 12. Simulation result of 2 input OR gate

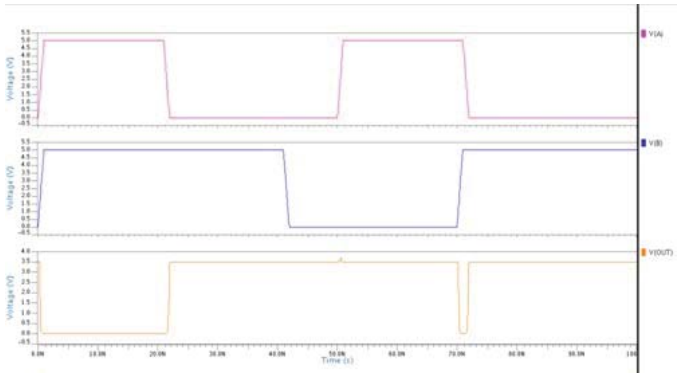

Figure 13. Simulation result of 2 input NAND gate

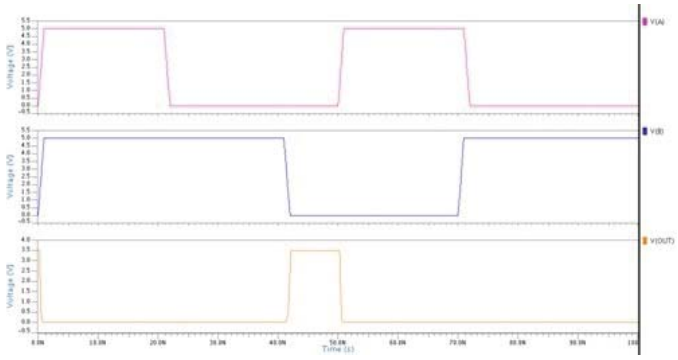

Figure 14. Simulation result of 2 input NOR gate

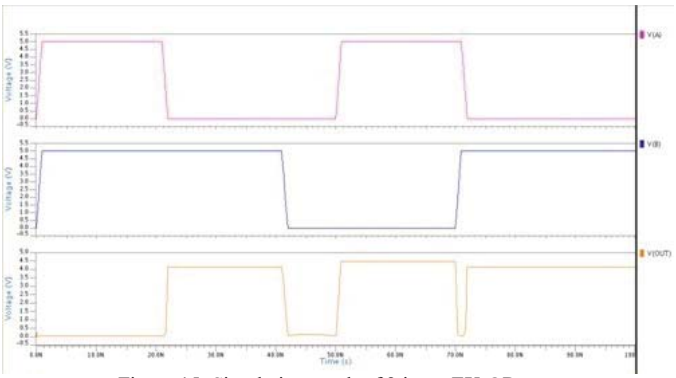

Figure 15. Simulation result of 2 input EX-OR gate

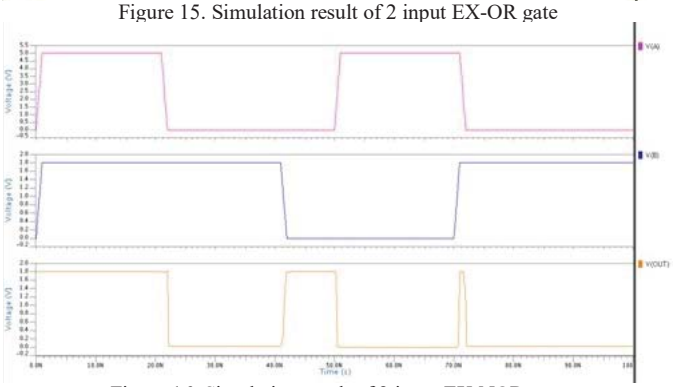

Figure 16. Simulation result of 2 input EX-NOR gate

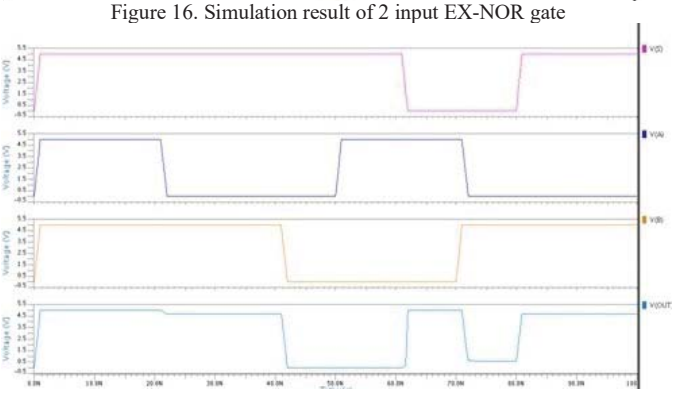

Figure 17. Simulation result of 2X1 Multiplexer

Table III. Comparison of total power dissipation with respective to all other techniques

Primitive Gates	Total power dissipation		
	CMOS in nw	GDI in nw	Mod-GDI in nw
INVERTER	30.23	9.20	9.20
AND	9.29	11.07	$6.48x10^{-5}$
OR	59.19	11.07	$647 x10^{-5}$
NAND	7.97	9.21	9.21
NOR	60.37	12.67	9.3
XOR	183.19	9.34	9.34
XNOR	183.89	20.28	5.83
2X1 Multiplexer	4.27x104	3.79	6.4 x10-5

Table V. Propagation delay of different logic functions

Primitive Gates	Propagation delay		
	CMOS In ns	GDI In ns	Mod- GDI In ns
INVERTER	20.7	20.8	19.25
AND	30.5	42.7	19.95
OR	29.69	48.7	18.08
NAND	20.57	76.13	16.49
NOR	40.97	19.0	19.0
XOR	102.5	78.3	29.15
XNOR	20.4	28.1	14.9
2X1 Multiplexer	49.87	20.06	8.4

Table IV. Transistor count of different logic functions

Primitive Gates	Transistor Count		
	CMOS	*GDI*	*Mod-GDI*
INVERTER	2	2	2
AND	6	2	2
OR	6	2	2
NAND	4	4	4
NOR	4	4	4
XOR	12	6	4
XNOR	14	6	6
2X1 Multiplexer	12	2	2

Table III shows the comparison of power dissipations among different design techniques like CMOS, GDI techniques. Total power dissipation for inverter is same in GDI and Mod-GDI cases because both the structure are same. All the proposed designs are operated at a low voltage of 1.8V which is allowed by Mod-GDI technique. The proposed designs are simulated at 90nm technology. From the table it is observed that total power dissipation of Mod-GDI designs is very low comparative to all other methods [1-2].

Similarly propagation delay for all the gate has been calculated and comparison between CMOS,GDI and Mod-GDI is tabulated in Table IV. Also total no. of transistors required to design the different logic gates is also shown in Table V.

V. CONCLUSIONS

The modified GDI cell was proposed and verified successfully. The proposed cell allow implementation of various logic functions, employing only two transistors and it is fully compatible for implementation in a standard CMOS process. Important features of Mod-GDI were presented. Simulation results, performed on basic logic gates were carried out in 90nm technology at very low voltage i.e., 1.8V.This shows the potential of the proposed method in advanced processes in total Power dissipation, Propagation delay and area calculations. Comparison results showing that Mod-GDI technique requires less power dissipation, low propagation delay and less no.of transistors than all other existing methods with very low supply voltage. With these less power dissipated gates, complex digital circuits can be implanted. Future work includes design and fabrication of more complex Mod-GDI structures.

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