Power Consumption in Combination Circuit by Using GDI Technology

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Abstract- An analysis of XOR gate designed using Gate Diffusion Input (GDI) technique is presented in this work. Comparative investigations are also carried out for XOR gates designed using conventional, low power as well as GDI techniques. SPICE simulations verify the results. The analysis shows that at 100MHz, circuit designed using GDI technique consumes 73.79%, 73.61%, and 46.64% less power compared to conventional, CPL and DPL technique. Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition. The vast use of this operation in arithmetic functions attracts a lot of researcher's attention to adder for mobile applications. In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells. These adder cells commonly aimed to reduce power consumption and increase speed. These studies have also investigated different approaches realizing adders using CMOS technology. For mobile applications, designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives. The designer's concern for the level of leakage current is not related to ensuring correct circuit operation, but is related to minimize power dissipation. For portable electronic devices this equates to maximizing battery life. For example, mobile phones need to be powered for extended periods (known as standby mode, during which the phone is able to receive an incoming call), but are fully active for much shorter periods (known as talk or active mode, while making a call).

Keywords – Gate Diffusion Input; DPL; CPL; XOR gate; GDI..

I. INTRODUCTION

The quick-tempered growth in portable digital systems, laptops and cellular networks has intensified the research efforts in low-power, high speed, compact implementation microelectronics circuit design. As VLSI technology scales down to nano regimes, it facilitates circuits with more and more functionality to be integrated in a single chip [1-3]. The battery technology does not advance at the same rate as the VLSI technology. There is a limited amount of power available for the mobile systems. Therefore, the integrated circuit (IC) designers encounter numerous constraints viz. high speed, high throughput, small silicon area, and at the same time low-power consumption. In order to improve the performance of logic circuits based on traditional CMOS technology has resulted in developing of new design techniques during the two last decades [4]. Adder is the core element of complex arithmetic circuits like addition, multiplication, division, exponentiation etc. Therefore building low-power, high performance adder cells are of great interest due to most of the VLSI applications, such as digital signal processing, image and video processing, and microprocessors, extensively use arithmetic operations [6]. XOR gate in turn becomes the essential part of the adder circuits. XOR gate has been analyzed in the present work using conventional and GDI techniques.

II. BRIEF LITERATURE REVIEW

For designing XOR gate there are various CMOS techniques like conventional CMOS, Complementary Pass Transistor Logic (CPL), Dual Pass Transistor Logic (DPL) etc. The Complementary Pass Transistor Logic (CPL) consists of NMOS pass transistor logic network driven by complementary inputs and CMOS inverters used as buffers. The inverting buffers translate the swing of the output from ground to VDD-Vth to a full-rail logic swing (ground to VDD). One drawback is associated with the CPL logic is the driving capability which is limited and delay increases with long pass transistor chains. So buffering is needed to restore the transmitted signal and improve the driving capability [7-9].

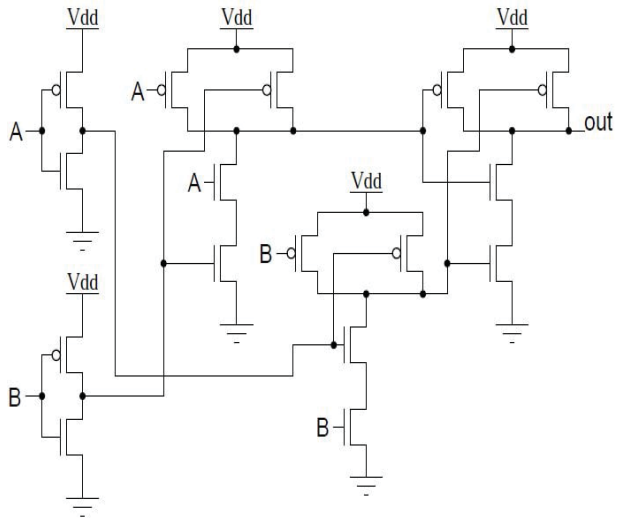

Fig.1. Conventional CMOS XOR Gate

Dual Pass Transistor Logic (DPL) is also based on the use of NMOS as logic gates, but uses additional transistors (PMOS) to overcome some of the electrical problem found in CPL. DPL also addresses loading problems that arise in the manner in which CPL uses signals. Compared to CPL, it uses twice as many transistors (& the associated increase in chip area) with more complicated interconnect wiring. Due to use of PMOS in DPL, an advantage to use DPL is ability to pass the power supply voltage VDD. The inputs to the DPL gate are (A, A') and (B, B') and that each variable is only used once. This means that the driving gates have equal loading and can be identical. CPL circuits do not have this characteristic. Full swing operation is obtained by simply adding PMOS transistors in parallel with the NMOS transistors in DPL circuits. Therefore, the problems of little noise margin and performance degradation at low supply voltages, which occur in CPL circuits because of the output voltage drop, are avoided. However, the addition of PMOS transistors bring about increased input capacitances

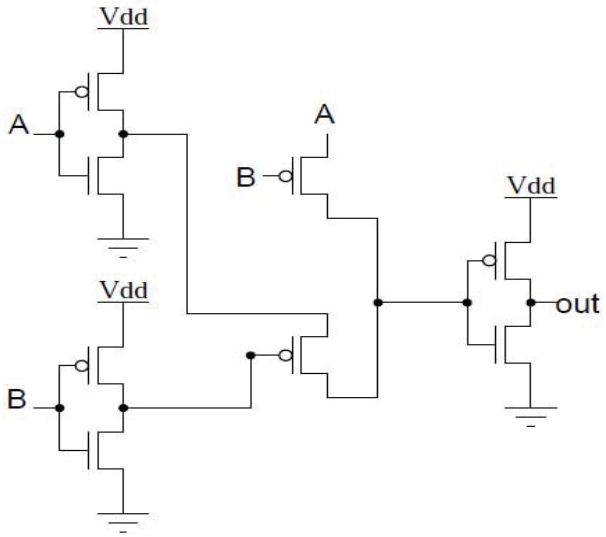

Fig 2 : CPL XOR Gate

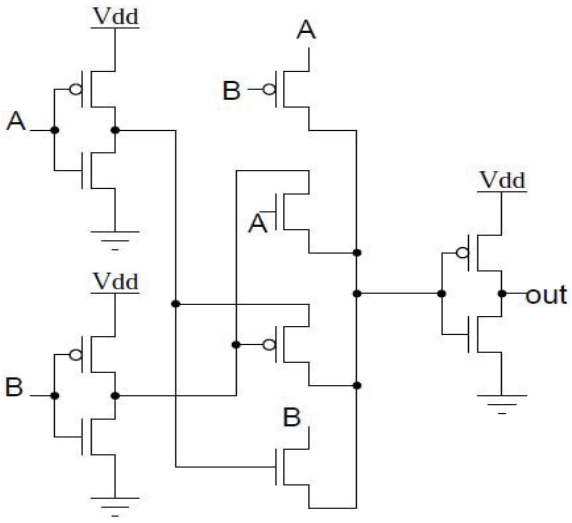

Fig 3 : DPL XOR Gate

III. GATE DIFFUSION INPUT TECHNIQUE

Before Gate Diffusion Input (GDI) method is based on the use of a simple cell as shown in Fig. 4 [11]. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences, GDI cell contains three inputs, G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). Bulks of both NMOS and PMOS are connected to N or P respectively [12]. By doing simple change in the input configuration of the simple GDI cell, different Boolean functions is obtained, e.g. AND, OR, MUX etc. Most of these functions are complex (6-12 transistors) in CMOS, as well as in standard PTLimplementations, but very simple (only 2 transistors per function) in GDI design method. XOR function is the key variables in adder equations. If the generation of them is optimized, this could greatly enhance the performance of the full adder cell [13-15].

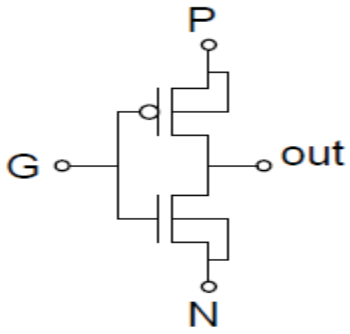

Fig 4 Basic GDI Cell

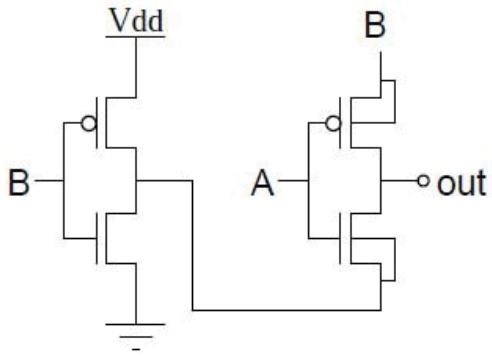

Fig 5 GDI XOR Gate

IV. RESULTS AND DISCUSSION

Performance investigations on various XOR circuits are presented in this section. Power debauchery (P), delay (D), power-delay-product (PDP), number of transistors (N) and power-delay-number-product (PDNP) are the performance metrics used for analysis. Analysis has been carried out using SPICE simulation [16]. Worst case delay and power dissipation have been considered in the present analysis. Fig. 6 shows the power dissipation of 2-input XOR gate for180nm technology, at 50MHz input frequency and 50fF load capacitance. All the four XOR gates are simulated for a voltage range of 1.2V to 3V. Power dissipation increases as the supply voltage increases. This is verified by the simulation results here. From Fig. 6, it is found that, GDI XOR gate has lowest power dissipation in the entire XOR gate simulated here. CPL XOR gate has highest power dissipation for the complete supply range taken for analysis.

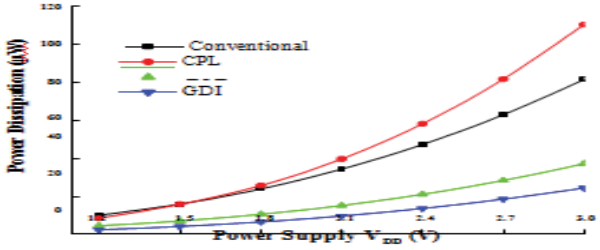

Fig.6. Variation of Power Dissipation with Power Supply in XOR Gate

Variation of gate delay with supply voltage of 2 input XOR gate is found out in Fig. 7. Fig. 7 shows that DPL XOR gate has lowest delay in all XOR gate analyzed here. The delay is also lower in GDI XOR gate. Delay is inversely proportional to the supply voltage. That means increasing the voltage, delay is reduced. This is verified by the simulation results here. The Power-Delay-Product is the main figure of merit to analyze the circuit. Fig. 8 gives the PDP (fJ) of 2 input XOR gate circuits. From the Fig. 8, it is found that DPL and GDI has lowest PDP factor in all XOR gates. Figure 9 shows the power dissipation variation with respect to frequency. Dynamic power (Pdy) as a function of frequency (f), load capacitance (CL) and supply voltage (VDD) can be given as [7]

$$P_{dy} = fC_LV^2_{DD}$$

It can be seen from (4.1) that dynamic power varies directly with frequency. Therefore with increasing frequency, the power dissipation increases. This is validated from the simulation results. From figure 9, it is concluded that, as frequency is increased, the power dissipation increases. GDI XOR gate has the lowest power dissipation at 100MHz frequency. Variation of gate delay with input frequency of 2 input XOR gate is found out in Fig. 10. shows thatDPL XOR gate has lowest delay in all XOR gate analyzed here. Fig. 11 gives the variation of PDP with input frequency of 2 input XOR gate circuits. From the Fig. 11, it is found that DPL and GDI has lowest PDP factor in all XOR gates.

Power increases with load capacitance. Also increasing the load capacitance increases the charging and discharging time. Hence it increases the delay and also the dynamic power dissipation. Hence increases the PDP. Fig. 12 shows the power dissipation variation with load capacitance at Supply voltage
1.8V, input frequency 50MHz are taken. Figure 13 shows the delay variation with load capacitance and Figure 14 shows the PDP variation with load capacitance at same condition as taken in Fig. 12. The transistor counts for 2 input XOR gate are shown in Fig. 15. It can be seen that GDI XOR gate has lowest transistor count, whereas conventional XOR gate has highest transistor count in comparison to other XOR gate analyzed here. Hence GDI XOR circuit is best choice in terms of chip area.

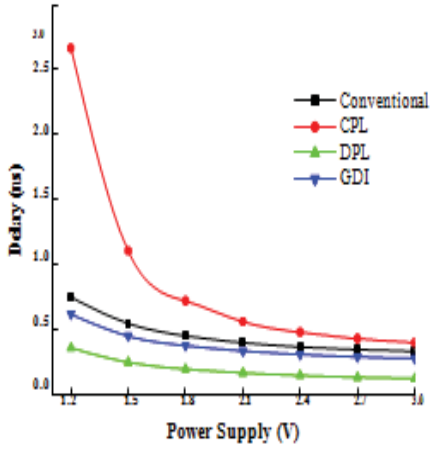

Fig.7. Variation of Gate delay with Power Supply in XOR Gate

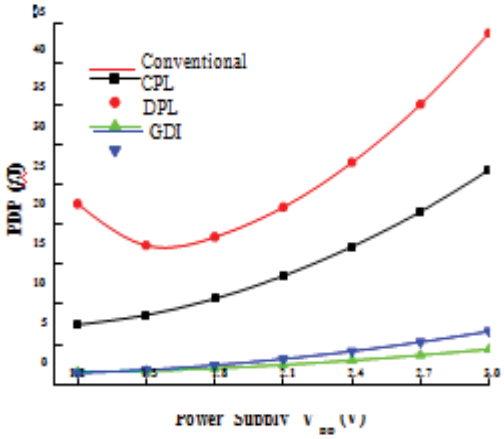

Fig.8. Variation of PDP with Power Supply in XOR Gate

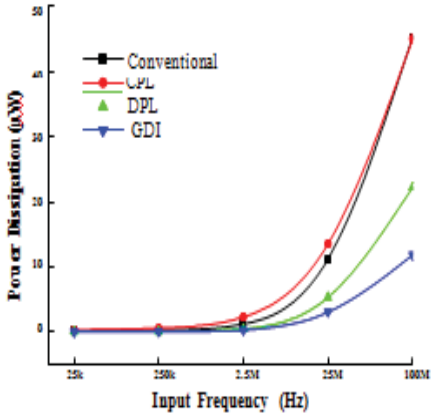

Fig.9. Variation of Power Dissipation with Input Frequency in XOR Gate

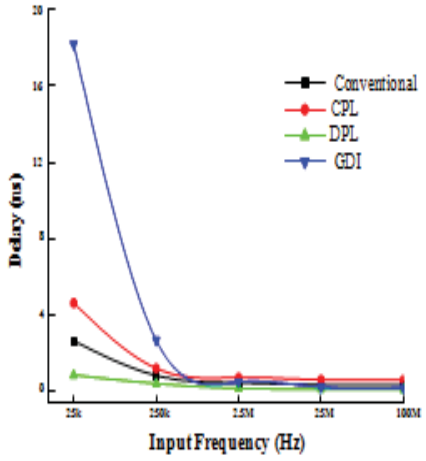

Fig.10. Variation of Gate Delay with Input Frequency in XOR Gate

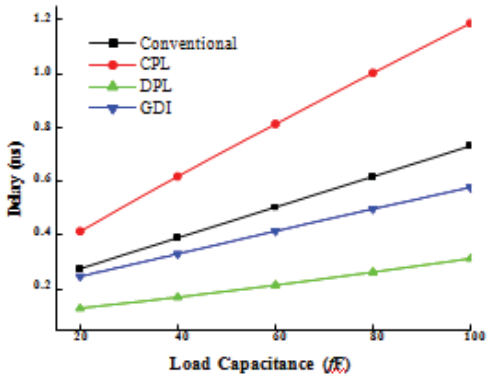

Fig.13. Variation of Gate Delay with Load Capacitance in XOR Gate

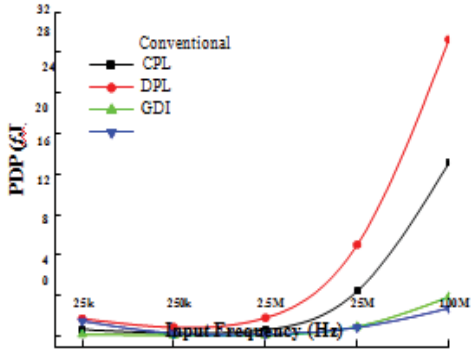

Fig.11. Variation of PDP with Input Frequency in XOR Gate

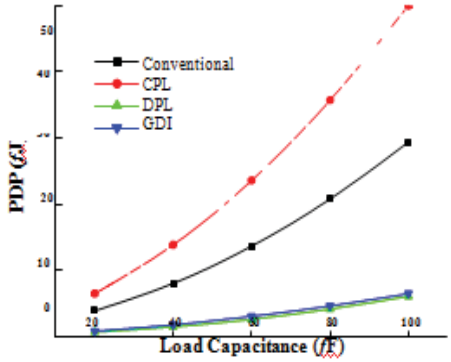

Fig.14. Variation of PDP with Load Capacitance in XOR Gate

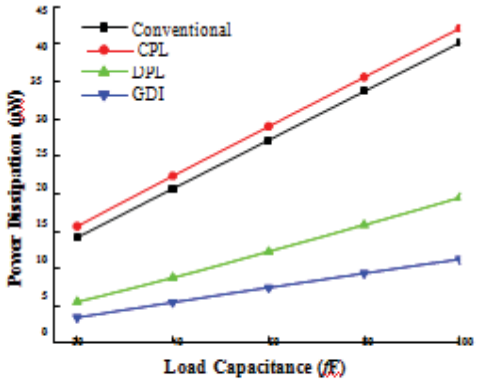

Fig.12. Variation of Power Dissipation with Load Capacitance in XOR Gate

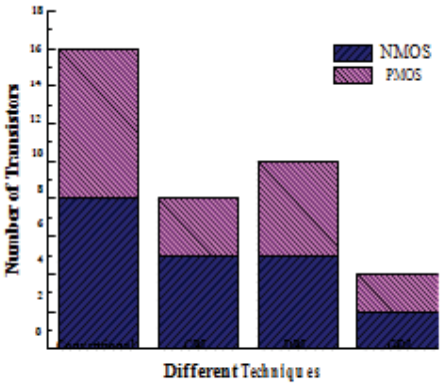

Fig.15. Number of transistors used in an XOR designed in different techniques

Parameters	Conventional	CPL	DPL	GDI
Transistor Count (N)	16	8	10	**4**
Area (μm^2)	3.1104	1.2636	1.944	**0.7776**
Delay (ns)	0.448	0.718	**0.193**	0.374
Power (W)	23.93	25.69	10.52	**6.49**
PDP (fJ)	10.73	18.43	**2.03**	2.43
PDNP (fJ)	171.68	147.44	20.3	**9.72**

Table I- COMPARATIVE ANALYSIS OF THE XOR DESIGNS V_{DD}= 1.8V, C_L= 50fF and *f*= 50MHz

Table I summarizes the comparative performance analysis of the XOR gates designed using four different techniques. Worst case analysis has been considered for comparison. Table I indicates that minimum number of transistors equal to 4 are required for XOR implementation in GDI technique It is shown bold in the last column II row of Table I. It can be seen that the area requirement for this XOR circuit is merely 0.7776

DPL technique shows power performance next best to GDI area advantage in GDI is at the cost of delay. Delay is least for DPL technique XOR and is 0.193ns. In terms of PDP the value for GDI is higher than DPL.Furthermore, PDNP is the main performance metric for the present analysis. Lower value of PDP ensures low energy consumption in a circuit. However, least PDNP leads to lowest energy as well as least chip area requirement. In the present analysis GDI has least PDNP value of 9.72fJ. Thus GDI XOR circuit has 52.12% lesser PDNP compared to DPL. This shall lead to a saving in silicon estate and thereby least cost of the circuit design.

V. CONCLUSIONS

XOR gate is implemented by using GDI and other low power techniques. The analysis shows that at 100MHz, circuit designed using GDI technique consumes 73.79%, 73.61%, and 46.64% less power compared to conventional, CPL and DPL techniques. Therefore, for power centric designs where stringent control of authority dissipation is essential, use of GDI technique will be the best choice amongst other techniques. The analysis shows that at100MHz, circuit designed using DPL technique has 53%,73.23% and 25.64% less delay compared to conventional, CPL and GDI technique. For delay centric design, use of DPL technique will be the best choice among other techniques. Now a day, chip area is very important parameter. With respect to chip area, GDI technique is significantly advantageous over other technique.

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