Analysis of 6T-SRAM Cell Designs Using MOS and FGMOS for Low Power Applications

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Abstract-SRAM (Static Random Access Memory) is a type of semiconductor memory that uses two cross coupled CMOS inverter to store each bit. It is the main part of cache, therefore its power dissipation reduction is the main concern. Last one decade has shown intensive research for reducing power dissipation and delay. The present work aims to reduce leakage power without affecting the logic state of SRAM cell. Power dissipation and delay, simulation in read and write operation of SRAM cell has been performed to analyze the results. Furthermore, analysis has been done for the SRAM cell by using forced stack transistor technique and sleep transistor technique. The simulation has been done using SPICE for 180nm, 90nm, 65nm, 45nm and 32nm CMOS technology nodes. The supply voltage 0.35V is used for sub threshold operation. Results indicate that use of FGMOS in place of MOS in SRAM cell reduces power dissipation and delay.

Keywords-MOS, FGMOS, Write delay, Read delay, Power Dissipation, Supply voltage.

I. INTRODUCTION

SRAMs are widely used for mobile application because of their ease of use and low power dissipation. The demand for low power devices has been increases tremendously in recent years. The aggressive scaling of CMOS device achieves higher density, improved performance and lower power consumption. Transistor delay time decrease per technology results doubling of performance. To keep the power consumption under control, the supply and threshold voltages have been scaled down. However, scaling of threshold voltage results in increasing of the sub threshold leakage current [1-2]. The threshold voltage and oxide thickness decreases when we decrease the supply voltage. Tremendous increase in device density and reducing threshold voltage results in vigorous increase in the leakage power.

Semiconductor memories have always been of interest to VLSI designers. It has been observed from literature that the bit-line parasitic capacitance increases when the memory capacity is increased which in turn slows down voltage sensing and depreciate the bit-line voltage swings energy. This results in slower and more energy greedy memories [2].

II. LITERATURE REVIEW

A. 6T-SRAM

Figure.1 shows the structure of the Basic six transistor 6T-SRAM. The memory cell consists of two cross coupled CMOS inverters, and two transistors to access. When a word line is activated the access transistors are turned on for read or write operation, which connect the memory cell to the complementary bit line columns. The power dissipation in this case is very high. Therefore, other design techniques are used for reducing the power dissipation [3].

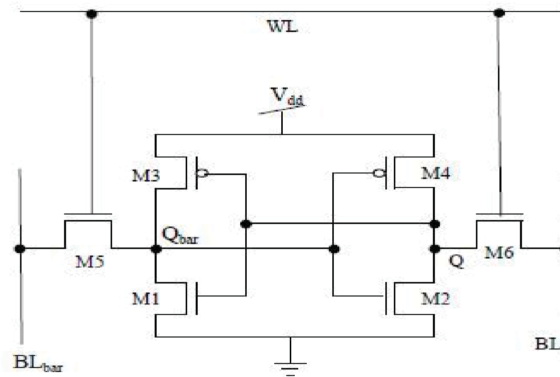

Figure1. Basic 6T-SRAM

B. SRAM With Sleep Transistor Technique

In the sleep transistor technique , the sleep transistor are used at two different position ,one pMOS transistor and one nMOS transistor in series with the transistors of cell so that virtual ground and virtual power supply is formed [4]. In active mode to make the circuit functions correctly, the sleep transistor is turned on, whereas in sleep mode the sleep transistor is turned off which makes the source nodes of the gates float and thus cutting off the leakage path. The power dissipation reduction is due to mainly 2 reasons- stacking of transistors and low sub-threshold leakage current of high Vth.

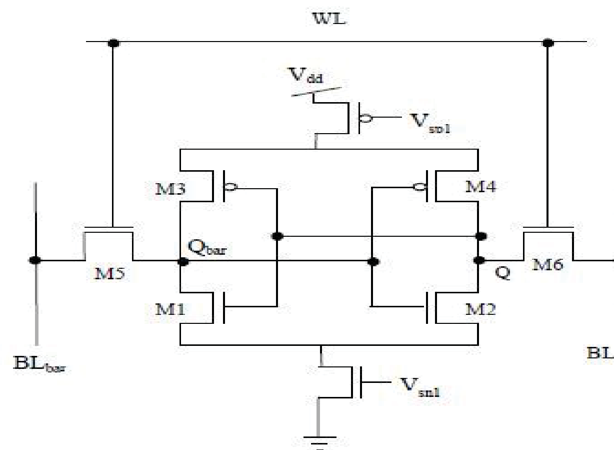

Figure 2. SRAM using sleep transistor technique

C. SRAM With Stack Technique

In this technique existing transistor is breakdown into two half size transistors. Figure 3 shows its structure. In stack technique when the both half size transistors are turned off simultaneously, reverse bias is induced between them which results in reducing the sub-threshold leakage current. However, due to divided transistors delay increases significantly which limits the usefulness of the approach. Wake-up overhead caused by sleep transistors is reduced by placement of alternating sleep transistors. Thus, number of sleep transistors used in the stack technique is less than that in the original sleep approach.

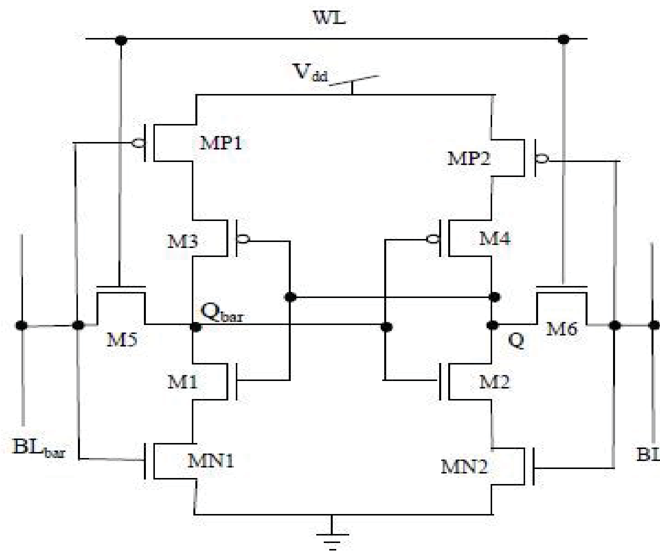

Figure 3. SRAM cell using forced stack transistor technique

III. SRAM DESIGN TECHNIQUES USING FGMOS

Figure 4, 5, 6 shows the circuit implementation of SRAM design techniques using FGMOS. This technique is basically normal MOS transistors only but with shifted threshold potential [6]. A capacitance connected to the gate of the MOSFET, also known as the floating gate capacitance, introduces the shift in the threshold potential by node voltage and hence decreases the power dissipation. Due to this, gate of the transistor is said to be floating.

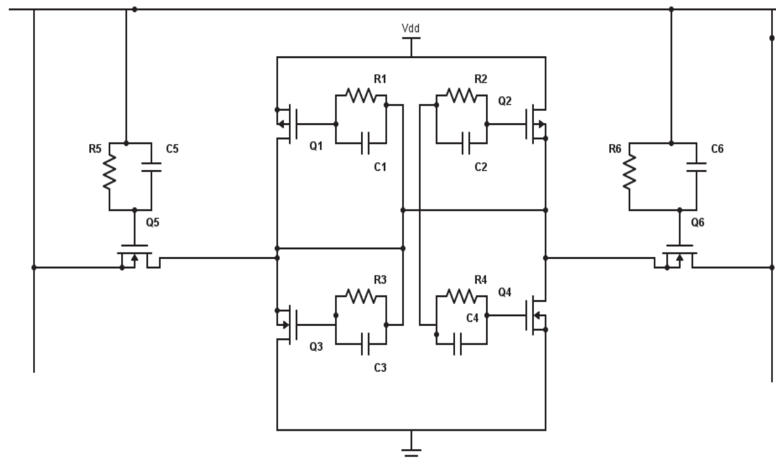

Figure 4. SRAM using FGMOS transistor technique

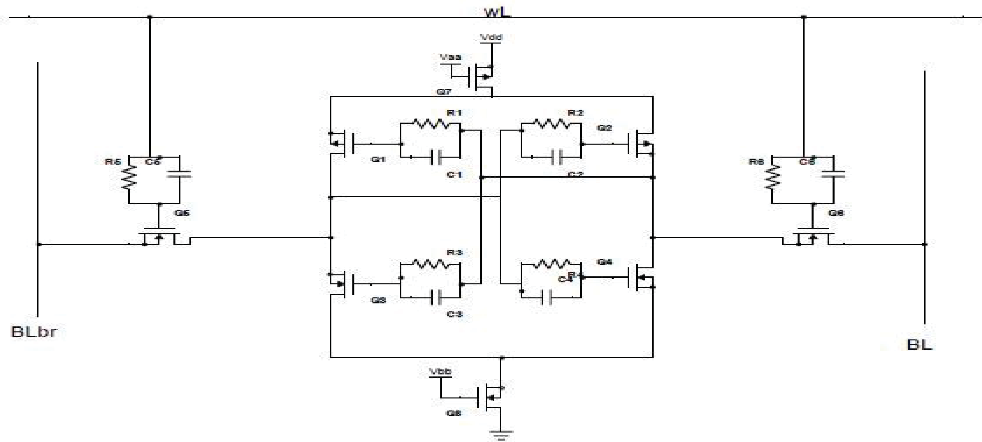

Figure 5. SRAM using FGMOS transistor technique with sleep transistor

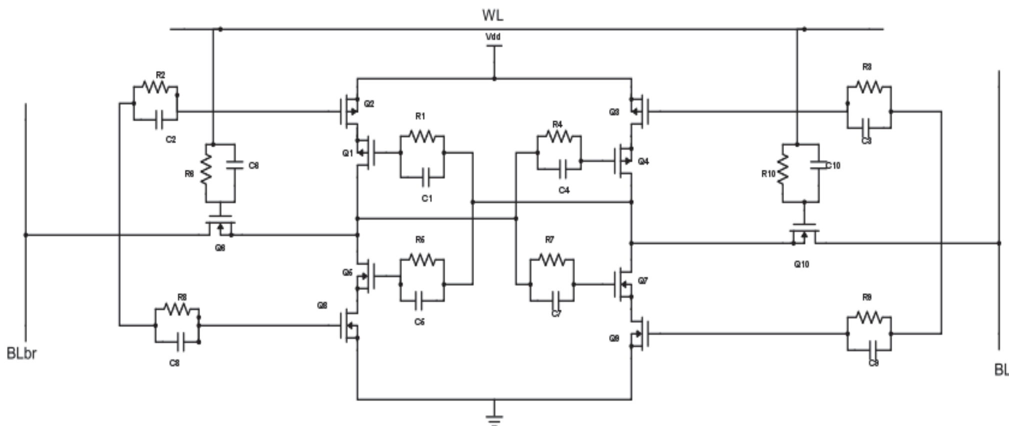

Figure 6. SRAM using FGMOS transistor technique with stack transistor

IV. RESULTS AND DISCUSSION

Simulations in this study are performed for 180nm, 90nm, 65nm, 45nm, and 32nm technology nodes using SPICE simulator. The results obtained for the power dissipation and delay analyses carried out during read and write operations in SRAM using MOS and FGMOS are presented in this section. To dealt with sub threshold operation we use V_{dd}=0.35V for all technology and techniques in this analysis . This reduces the power dissipation, making the SRAM cell applicable for low power applications, and the use of FGMOS further decreases the power dissipation and delay of the SRAM cell.

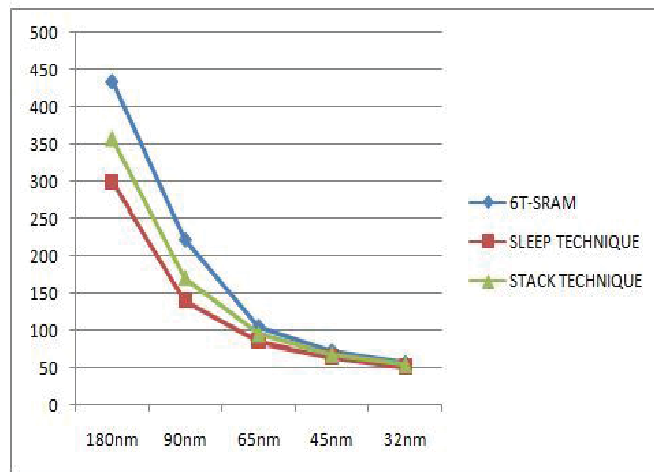

Figure 7. Power dissipation verses different technology nodes for various techniques using MOS.

From the above figure, it is seen that the basic 6T-SRAM cell consumes more power as compared to sleep technique and forced stack technique. It is also seen that sleep technique has least power dissipation compared to the other techniques. So in terms of power dissipation, sleep technique gives us the best performance.

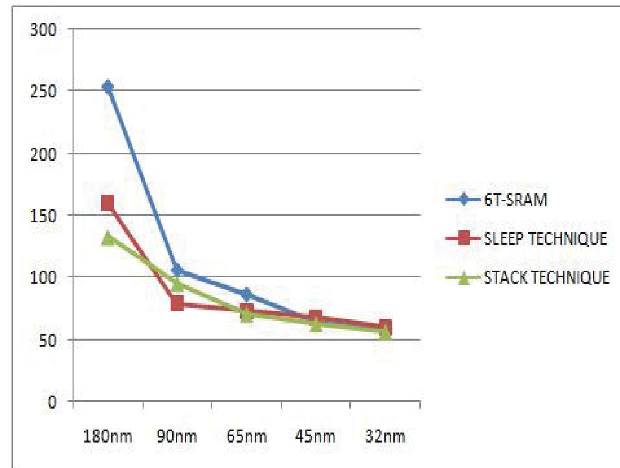

Figure 8. Power dissipation verses different technology nodes for various techniques using FGMOS.

Figure 8. shows the power dissipation variation for the three SRAM design techniques using FGMOS. From the figure, it is seen that the basic 6T-SRAM cell consumes more power as compared to sleep technique and forced stack technique. It is also seen that in most of the technology nodes the forced stack technique has least power dissipation compared to the other techniques. So when we use FGMOS in place of MOS forced stack technique gives us the best performance. Moreover from figure 7 and figure 8, we can see that the use of FGMOS in place of MOS in SRAM decreases the power dissipation and increases the performance.

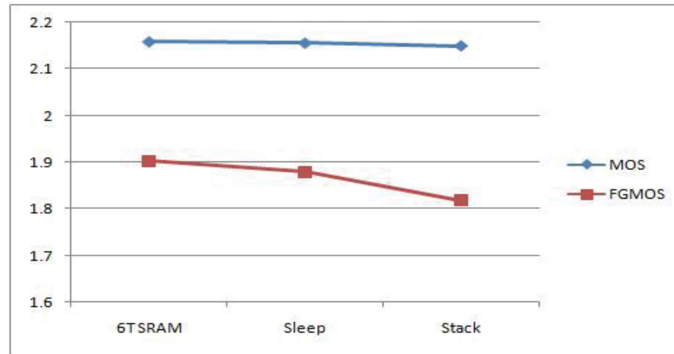

Figure 9. Delay variation for the three SRAM cell design techniques using MOS and FGMOS during read operation (180nm).

Figure 9. Shows the read delay variation for the three techniques using MOS and FGMOS in 180nm technology node. From the figure, it is seen that techniques using FGMOS shows considerable decrease in read delay as compared to techniques using MOS. Among different techniques 6T-SRAM and sleep technique has more read delay as compared to stack design techniques for SRAM cell.

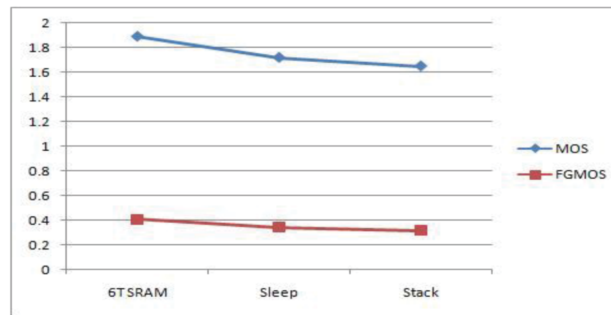

Figure 10. Delay variation for the three SRAM cell design techniques using MOS and FGMOS during write operation (180nm).

Figure 10. Shows the write delay variation for the three techniques using MOS and FGMOS in 180nm technology node. From the figure, it is seen that techniques using FGMOS shows considerable decrease in write delay as compared to techniques using MOS. Among different techniques 6T-SRAM and sleep technique has more write delay as compared to stack design technique for SRAM.

TABLE I: POWER DISSIPATION FOR VARIOUS TECHNIQUES USING MOS (nW)

Technology nodes	**6T-SRAM**	**SLEEP**	**STACK**
180nm	371	**277**	341
90nm	223	**141**	171
65nm	106	**86.3**	95
45nm	73.2	**64**	68
32nm	57.0	**51.5**	54

Table-I shows the power dissipation for various techniques using MOS in active mode and it can be seen that as compared to other techniques sleep gives the least power dissipation. For example, average power dissipation is 277nW, 141nW, 86.3nW, 64nW and 51.5nW for 180nm, 90nm, 65nm, 45nm and 32nm technology nodes respectively which is much less than the power dissipation for 6T-SRAM and forced stack technique.

TABLE II: POWER DISSIPATION FOR VARIOUS TECHNIQUES USING FGMOS (nW)

Technology nodes	6T-SRAM	SLEEP	STACK
180nm	254	160	**133**
90nm	106	79.2	**95**
65nm	86.3	73.2	**70.2**
45nm	64	68.2	**62.4**
32nm	57.1	60.2	**55.8**

Table-II shows the power dissipation for various techniques using FGMOS in active mode and it can be seen that forced stack technique gives the least power dissipation as compared to other techniques.

TABLE III: DELAY DURING READ OPERATION FOR VARIOUS TECHNIQUES USING MOS AND FGMOS FOR 180nm TECHNOLOGY

SRAM design techniques using MOS	Read delay (us)	SRAM design techniques using FGMOS	Read delay (us)
6T-SRAM	2.158264	**6T-SRAM**	1.9026
SLEEP	2.1554	**SLEEP**	1.879
STACK	2.149164	**STACK**	1.8182

TABLE IV: DELAY DURING WRITE OPERATION FOR VARIOUS TECHNIQUES USING MOS AND FGMOS FOR 180nm TECHNOLOGY

SRAM design techniques using MOS	Write delay (us)	SRAM design techniques using FGMOS	Write delay (us)
6T-SRAM	1.889	**6T-SRAM**	0.409
SLEEP	1.719	**SLEEP**	0.3446
STACK	1.65	**STACK**	0.319

Table-III shows the delay for read operation for various techniques using MOS and FGMOS for 180nm technology node and Table-IV shows the delay for write operation for various techniques using MOS and FGMOS. From these two tables it can be observed that forced stack technique shows the least read and write delay as compared to 6T-SRAM and sleep technique and also that the use of FGMOS in place of MOS considerably decrease the read and write delay.

V. CONCLUSIONS

In the present work the power dissipation is computed for different SRAM cell design techniques using MOS and FGMOS. Sub threshold operation is performed which helps to attain low power applications. It has been observed that sleep transistor technique shows minimum power dissipation as compared to the conventional 6T-SRAM cell and stack transistor technique when we use MOS and when we use FGMOS the stack transistor technique shows minimum power. In case of delay measurement, it is observed that stack transistor technique provides the least delay in comparison to the conventional 6T-SRAM and sleep transistor technique using MOS and FGMOS. We can see that the use of FGMOS in place of MOS considerably decreases the power dissipation and delay of the SRAM cell.

Thus, simulation result provides that using FGMOS in place of MOS decreases power dissipation and delay, therefore SRAM using FGMOS can be preferred. Moreover the power dissipation of sleep transistor technique and

smallest average delay of stack transistor technique shall be used to design a new SRAM circuit technique using MOS to enhance the overall performance and in case of FGMOS we shall go for stack transistor technique as it has least power dissipation and delay and hence the overall performance can be enhanced.

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