A Comparative Study of 6T, 8T and 9T Sram Cell

Deepak Aggarwal  
Student, BRCM College, Bahal

Praveen kaushik  
Student, Manav Bharti University, Solan

Narender Gujran  
Assistant Prof., BRCM College, Bahal

Abstract: From last 5 decades, we are scaling down the CMOS devices to achieve the better performance in terms of speed, power dissipation, size and reliability. Our focus is to make the general use device like computer more compact in terms of size, better speed, less power consumption and so we are moving towards the new technology. That can be done by making memories compact and faster and so the scaling CMOS is done to attain high speed and decrease size of memory i.e. SRAM. Due to scaling of device we are facing new challenges day by day like oxide thickness fluctuation, intrinsic parameter fluctuation. Working on low threshold voltage and leakage energy also became main concern. SRAM (Static Random Access Memory) is memory used to store data. The comparison of different SRAM cell on the basis of different parameter is done. 6T, 8T and 9T SRAM cell are compared on basis of followings: 1) Read delay, 2) Write delay, 3) Power dissipation. The technology used to implement the 6T (T stands for transistor), 8T and 9T SRAM is 90 nm technology and the software used is ORCAD PSPICE. Schematics of these SRAM have been implemented using ORCAD CAPTURE and analysis is done using PSPICE A/D tool of ORCAD PSPICE.

1. INTRODUCTION

The dissertation work revolves around the performance comparison of SRAM cells consisting of different number of transistors used to store single bit. SRAM stands for static random access memory. It is a type of semi-conductor memory which uses bi-stable latching circuitry to store single bit [1]. The word static here points that it needs not to be refreshed periodically unlike dynamic random access memory. Sram exhibits data-remanence but still it can be called volatile memory as it eventually loses the data when memory is not powered [2].

From last four decades, we are scaling down the CMOS devices to achieve the better performance in terms of speed, power consumption, noise margins, delay etc. Sram based cache memories are commonly used due to their higher speed. But due to device scaling we are facing design challenges for nanometre sram design. Because of low threshold voltage and ultra thin gate oxide, the leakage energy consumption is getting increased. The data stability during read and write operation is also getting affected [5]. There are some other factor like random dopant fluctuation, line edge roughness and oxide thickness fluctuation.
which decreases the stability of sram cell [3]. In this dissertation performance analysis of 6T, 8T and 9T has been carried out based on read delay, write delay and power consumption.

II. DESIGN OF SRAM CELLS

6T SRAM cell Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control access to a storage cell during read and write operations [6]. A typical SRAM uses six MOSFETs to store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 8T, 10T, or more transistors per bit. Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL bar [7]. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins.

![Fig. 1. A 6T SRAM Circuit](image)

An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents[8]. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows:

2.1 STANDBY

If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

2.2 READING

Assume that the content of the memory is a 1, stored at Q. The read cycle is started by pre-charging both the bit lines to a logical 1, then asserting the word line WL, enabling both the access transistors. The second
step occurs when the values stored in Q and Q bar are transferred to the bit lines by leaving BL at its precharged value and discharging BL bar through M1 and M5 to a logical 0. On the BL side, the transistors M4 and M6 pull the bit line toward VDD, a logical 1. If the content of the memory were a 0, the opposite would happen and BL would be pulled toward 1 and BL toward 0. Then these BL and BL-bar will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was 1 stored or 0. The higher the sensitivity of sense amplifier is faster is the speed of read operation of SRAM.

2.3 WRITING

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BL to 0. This is similar to applying a reset pulse to a SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell i s needed to ensure proper operation.

We can see from the figure that M5 and M6 transistor are connected to write line and M7 and M8 transistor are connected to read line and also these transistors are high voltage transistor that means threshold voltage is higher for these transistors as compared to normal transistor. The difference between is more visible in figure 4.4. the gate line is bold in case of high voltage NMOS transistor. In case of 9T SRAM, M7, M8, M9 all are high-vt transistors.

For the implementation the technology being used is 90 nm [15]. The key features of 90 nm technology in comparison to 130 nm technology are:-

- At standard transistor, 25% faster (gate level).
- Transistor density is doubled compared with the 130nm generation
- SRAM cell area reduced by 50%.
The transistors used in SRAMs are based on 90 nm technology. Length of each transistor is taken 90 nm and width of transistor is variable for different transistors. For example the transistors used in CMOS inverter have the width 120 nm. These are shown in table1 to table 3 for 6T, 8T & 9T SRAM respectively [11,12,13,14].

### TABLE 1 - WIDTH OF TR. USED TO SIMULATE 6T SRAM CELL

<table>
<thead>
<tr>
<th>TRANSISTOR</th>
<th>WIDTH (in nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1,M2,M3,M4</td>
<td>120</td>
</tr>
<tr>
<td>M5,M6</td>
<td>600</td>
</tr>
</tbody>
</table>

### TABLE 2 - WIDTH OF TR. USED TO SIMULATE 8T SRAM CELL

<table>
<thead>
<tr>
<th>TRANSISTOR</th>
<th>WIDTH (in nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1,M2,M3,M4</td>
<td>120</td>
</tr>
<tr>
<td>M5</td>
<td>600</td>
</tr>
<tr>
<td>M6</td>
<td>240</td>
</tr>
<tr>
<td>M7,M8</td>
<td>480</td>
</tr>
</tbody>
</table>

### TABLE 3 - WIDTH OF TR. USED TO SIMULATE 9T SRAM CELL

<table>
<thead>
<tr>
<th>TRANSISTOR</th>
<th>WIDTH (in nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1,M2,M3,M4</td>
<td>120</td>
</tr>
<tr>
<td>M5,M6</td>
<td>600</td>
</tr>
<tr>
<td>M7,M8</td>
<td>240</td>
</tr>
<tr>
<td>M9</td>
<td>480</td>
</tr>
</tbody>
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### IV. SRAM IMPLEMENTATION

6T, 8T and 9T SRAM structure are implemented on the PSPICE and the graph for the read delay, write delay and power dissipation are obtained using PSPICE A/D analysis [4].
Fig 4 - 6T SRAM CELL WRITE MODE GRAPH

Fig 5 - 6T SRAM CELL READ MODE GRAPH
Fig 6: 8T SRAM CELL WRITE MODE GRAPH

Fig 7: 8T SRAM CELL READ MODE GRAPH
V. RESULTS AND CONCLUSION

The final results for the read delay, write delay and power dissipation are shown in table 4.4 and 4.5.
In this paper, the whole text has been concluded and we got the all results as follows:

After comparing the 6T and 8T SRAM cell, it is found that 6T sram cell provide a very low write delay nearly 7 times lesser when compared to 8T SRAM cell. While in case of read delay there is less difference, read delay of 8T SRAM is nearly 1.35 times higher as compared to 6T SRAM. The power dissipation of 6T sram is half of power dissipated in 8T SRAM. This is due to more number of transistor in 8T SRAM and secondly little complex working than other one. In case of 9T SRAM the write delay as compared 6T SRAM is nearly equal. The width of the transistor also affects the delay but we can’t extend width too much as it increases the area of the SRAM cell. While talking about the results of 9T SRAM, we see that the read delay of this SRAM is little bit high as compared to 8T SRAM and nearly 1.45 higher than 6T SRAM’s read delay. Read delay is maximum in case of this cell because it uses the high voltage transistor which increases the delay but it improves the driving capability. Performance is improved in case of this cell. If we notice the write delay, it is almost equal to 6T SRAM write delay. The 9T SRAM structure uses the advantages of 6T and 8T SRAM, 9T SRAM uses the two bit lines and also have the different read and write line. From results it looks like that 6T SRAM is the better one out of three but that is not right. Because there some other factor also on which performance of these cell depends. Data retention voltage is one out them. From the theoretical study and literature survey it is found 9T SRAM have low data retention voltage out of three cells.

VI REFERENCES


[12] Robert J. Hofinger, Purdue University “OrCad Capture Release 15.7” 2008.

